Design and fabrication of PCR chip with integrated dielectrophoretic based sample pretreatment

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Design and Fabrication of PCR Chip with Integrated Dielectrophoretic Based Sample Pretreatment

Ph.D. Thesis
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Preface

This thesis has been written as a partial fulfillment of the requirements for obtaining the Ph.D. degree at the Technical University of Denmark (DTU). The research for the Ph.D. project has been conducted at Mikroelektronik Centret (MIC) at DTU in the period from March 2000 to February 2003.

The Ph.D. project has been carried out in the cell/particle handling project under the supervision of the following people:

Project leader, Dr. Anders Wollf, main supervisor
Director of MIC, Professor Pieter Telleman, co-supervisor
Associate Professor Ole Hansen, co-supervisor

The project has mainly been financed by a grant from DTU within the electrical engineering programme.

Many people have contributed to and have been involved in the 3 years work of this project. I would like to thank my main supervisor, project leader Anders Wolff for his enthusiastic involvement in the project. A special thanks goes to my co-supervisor Ole Hansen for his creative ideas and suggestions, both within the field of process development, but especially for his help and guidance towards understanding the basic physical behavior of the components. I would also like to thank Pieter Telleman for his guidance when results has to be put in writing.

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Finally I wish to thank my family and friends for their support during my project.

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Abstract

Micro total analysis systems (μTAS) ideally integrates all steps from sample preparation to data representation of the analysis into one microfabricated system. Sample pretreatment performed on microfabricated devices is still under development and is one of the main challenges that remain in the development of true μTAS. This thesis deals with the integration of a dielectrophoretic (DEP) based sample pretreatment system with a polymerase chain reaction (PCR) microchip. The integration is achieved by development of designs that uses the photoresist SU-8 to define all the fluidic components of the two systems on glass substrates.

First a PCR chip design was developed with a SU-8 based PCR chamber fabricated on a glass substrate. Integrated thin film heater and temperature sensor electrodes control the PCR thermocycling. Simulations and measurements showed that the PCR chip design was capable of fast thermocycling with heating and cooling rates in excess of 50°C/s and 30°C/s, respectively. When the PCR compatibility of the chamber surfaces was enhanced by silanization the yield of the PCR chips were up to 2/3 of the yield using conventional PCR tubes.

The DEP based sample pretreatment system was based on designs with titanium and nickel silicide electrodes fabricated on various substrates with a simple SU-8 fluidic system. It was shown that DEP devices could be used to perform a number of typical sample pretreatment tasks like separation and concentration of cells.

Based on the developed components an integrated device was designed and fabricated. The DEP based sample pretreatment system was connected to the PCR chamber using a fluidic system that allows the sample pretreatment to be performed in a separate medium than the PCR amplification. Initial testing of the integrated chip was performed on a sample with yeast cells and a known amount of heparin, which inhibits PCR. It was found that only the treated sample was successfully amplified.

SU-8 based polymer waveguides were also developed using a fabrication process compatible with the integrated PCR chip. The waveguides had a relatively high propagation loss at wavelengths below 550nm. However, above 550nm the loss was less than 3db/cm. The functionality of the waveguides were tested in a flow cytometry setup using fluorescent beads.

Resume (in Danish)

Mikro total analyse systemer (μTAS) integrerer ideelt set alle analyse trin fra prøve forberedelse til dataopsampling i et samlet mikro-fremstillet system. Prøve forberedelse udført i mikrosystemer er stadigvæk under udvikling og det er en af de store udfordringerne i udviklingen af rigtige μTAS. Denne afhandling omhandler integration af et dielectroforetisk (DEP) baseret system til prøve forberedelse med en mikro-fabrikeret PCR (polymerase chain reaction) chip. Integrationen er opnået ved at udvikle designs der definer alle fluide komponenter i de to systemer på glas substrater ved hjælp af fotoresisten SU-8.

Først blev en PCR mikrochip udviklet, baseret på et kammer fremstillet i SU-8 på glas substrater. Integrerede tyndfilms varme og temperatur følende elektroder kontrolerer temperatur cyklingen til PCR. Simuleringer og målinger viste at PCR chippen var i stand til hurtig temperatur cykling med varme og køle rater på op til henholdsvis 50°C/s og 30°C/s. Udbyttet i PCR chipsene var op til 2/3 af udbyttet opnået med konventionelle PCR rør når PCR kompatibiliteten af overfladerne i kammeret blev forbedret med en silanisering.

Det DEP baserede system til prøve forberedelse bygger på designs med titanium og nikkel silicid electroder fremstillet på en række substrater sammen med et simpelt SU-8 fluid system. Det blev vist at DEP systemerne kunne udføre en række af de typiske prøve forberedelses trin, som seperation of opkoncentrering af celler.

Et integreret design baseret på de udviklede komponenter blev designet og fremstillet. Det DEP baserede system til prøve forberedelse blev tilsluttet PCR kammeret ved hjælp af et fluid system der tillader at prøve forberedelsen finder sted i en anden væske end den der bliver brugt til PCR. Indledende test af det integrerede system blev udført med en prøve af gær celler indeholdende heparin, som inhiberer PCR. Kun den behandlede prøve blev succesfuldt amplificeret.

SU-8 baserede polymer bølgeledere blev også udviklet, med en fabrikations proces der er kompatibel med den integrerede PCR chip. Bølgelederne havde relativt højt udbredelses tab ved bølgelængder under 550nm. Derimod var udbredelses tabet mindre end 3dB/cm over 550nm. Funktionaliteten af bølgelederne blev testet i et flowcytometer setup ved hjælp a fluorescerende partikler.

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Abbreviations

AC : Alternating current
BHF : Buffered hydrofluoric acid
DNA : Deoxyribonucleic acid
CTE : Coefficient of thermal expansion
DEP : Dielectrophoretic/Dielectrophoresis
DI : De-ionized
FEM : Finite Element Modelling
HMDS : Hexamethyldisilazan
IR : Infrared
ITO: Indium tim oxide
LCD : Liquid crystal display
LPCVD : Low pressure chemical vapor deposition
μTAS : micro Total Analysis System
n-DEP : Negative Dielectrophoresis
PCR : Polymerase Chain Reaction
p-DEP : Positive Dielectrophoresis
PDMS : Polydimethylsiloxane
PECVD : Plasma enhanced chemical vapor deposition
PGMEA : Propylenglycolmonomethyletheracetat
PMMA : Polymethylmethacrylat
RIE : Reactive ion etching
ROT : Electrorotation
RTA : Rapid thermal anneal
rpm : Revolutions per minute
SIMS : Secondary ion-mass spectroscopy
SOG : Spin-on-Glass
TCR : Temperature coefficient of resistance
TE : Thermoelectric
TWD : Travelling wave Dielectrophoresis
UV : Ultra violet

List of symbols

α : Temperature coefficient of resistance (TCR)
α_r : Effective polarisability
c : Specific heat capacity
ε : Permittivity
ε^* : Absolute permittivity
h : Heat transport coefficient(convection)
λ : Thermal conductivity
n : Refractive index
P : Power
$\dot{Q}$: Heat transport
R : Radius
r : Radius
ρ : Density
σ : electrical conductivity
T : Temperature
t_i : Thicknesses
t : Time
ω : Angular frequency

Chapter 1

Introduction

The interest in microfabricated devices for biochemical analysis has increased rapidly during the last decade. The ultimate goal is to miniaturize a whole laboratory and integrate it onto a microchip, a so called micro total analysis system (μTAS) [1, 2]. A μTAS ideally integrates all steps from sample preparation to data representation of the analysis. The basic concept behind a μTAS system is shown in figure 1.1. It consist of a sample pretreatment system, a micro fluidic system, a detector system and an electronic interface for control and readout. The systems can be integrated in one chip, called monolithic integration, or consist of subsystems that have been realized separately and then assembled to form a complete system. The latter is called hybrid integration and is the method used in most μTAS devices developed so far.

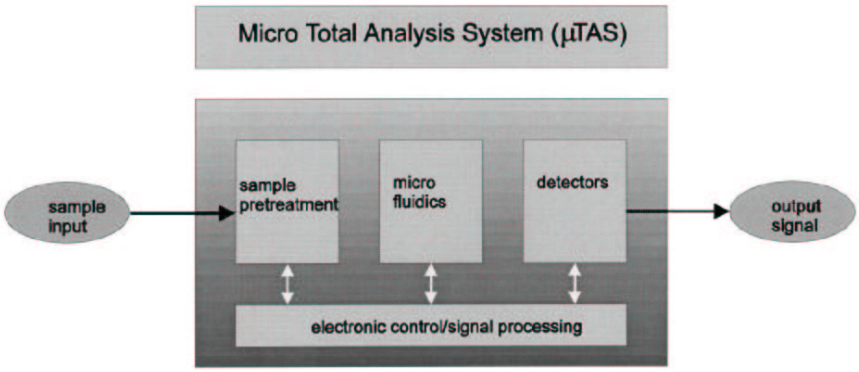

Figure 1.1: *Schematic of the μTAS principle. Ideally all step of an analysis, from sample preparation to detection and readout, is integrated into one system.[3]*

The sample pretreatment system conditions the sample so it is suitable for further analysis. This can involve extraction of the sample, filtering and removal of unwanted components, sample pre-concentration, or labelling of sample for detection purposes [4]. Although several devices and methods for sample pretreatment have been developed [5, 6, 7, 8] the area of sample pretreatment is still under development and is one of the main challenges that remain in the development of true μTAS [4].

The task of the microfluidic system is to control the movement of sample and reagent through the device. This is done using pumps and valves. Several pumps have been presented, both non-mechanical [9, 10, 11] and mechanical types [12, 13], but especially mechanical pumps have yet to be monolithically integrated in μTAS.

The job of the detector is to measure the desired quantity in the sample. Several different sensing techniques exist, including electrochemical [14, 15], electro mechanical [16], fluorescent [17, 18] and many others [19].

Although progress is constantly made, development of a true μTAS device has yet to be realized. Many of the presented devices only include a few of the functionalities required for analysis on chip. Most of the sample pretreatment takes place off chip, external pumps are often used for the fluidic handling, the detection system may use one or more external components and the electronics is handled by a computer and not on chip.

1.1 PCR on microchips

In this thesis the design and fabrication of a polymerase chain reaction (PCR) microchip with a monolithically integrated sample pretreatment system will be presented. PCR is an often used method for amplification of DNA, which is required in many DNA analysis systems. PCR microchips can be combined with other devices for sample pretreatment and post PCR analysis to form a complete μTAS device. Most work dealing with integration of PCR have so far focused on integration with post PCR analysis. The emphasis in this thesis will be on integration of PCR with a sample pretreatment system.

The polymerase chain reaction is an enzymatic method to amplify DNA by repeating a series of thermally controlled reaction steps [20]. There are 3 steps during a PCR thermocycle. Melting of the double stranded DNA, called denaturation, at an elevated temperature where the complementary strands in the DNA double helix separate. Binding of specific primers to a target site in a DNA strand at a lower temperature, called annealing, and finally extension of the primers at an intermediate temperature by a thermostable polymerase such as *Taq*. The number of amplified DNA molecules is ideally doubled during each cycle. Typical temperatures for the denaturation, annealing and extension steps are 94°C, 40-72°C and 72°C, respectively. In conventional PCR the thermocycling is done in a bench top system with the sample positioned in polypropylene tubes. Typical heating and cooling rates are up to 2-4°C/s

Integrating PCR onto micro fabricated devices can offer several important advantages compared to conventional PCR systems. The low thermal mass of these systems allows for fast heating and cooling rates, enabling faster thermocycling than possible

with conventional thermocyclers. This can lead to significant shorter amplification times and reduce the overall analysis time. Reduction of reagent volume will decrease the cost of the analysis, while reductions in size and power consumption of the device can make portable use possible. Furthermore, use of micro fabrication techniques can allow on chip integration with other functionality.

1.1.1 Silicon micromachined PCR chips

In 1993 Northrup *et al.* [21] reported the first example of a silicon microfabricated PCR chip. The chip had a 25-50μL PCR reaction chamber fabricated using silicon micro machining techniques, and had built in polysilicon heaters for the PCR thermocycling. The heaters were thermally isolated from the substrate by placing them on a silicon nitride membrane formed during the chamber fabrication. This reduces the power consumption of the device. The chamber was sealed by bonding of a lid. A schematic of a typical silicon based PCR chip is shown in figure 1.2. The reported heating rate for the 25μL chip was in excess of 35°C/s with similar cooling rates and thus much faster than conventional PCR thermocyclers. Using a similar design but with 5-10 μL reaction chambers Poser *et al.* [22] reported heating and cooling rates up to 80°C/s and 40°C/s, respectively. A fan was incorporated in that system to enhance the cooling rate of the device. The power consumption at 94°C was 1,25W. In the design of Daniel *et al.* [23] where the PCR chamber volume was only a few μL heating rates, depending on the input power, as high as 60-90°C/s was obtained, with cooling rates of more than 70°C/s. The power consumption at 90°C was $\sim$2W.

Temperature uniformity and temperature control are some of the major requirements in the design of a PCR chip, because the strong temperature dependence of the PCR reaction [25]. In a design similar to Northrup with a 20μL bulk silicon micro machined PCR chamber and with integrated thin film heaters fabricated on a nitride membrane, Lao *et al.* [26] investigated the temperature homogeneity in the PCR chamber using 3D finite element modelling. They found that the temperature distribution in the middle of the PCR chamber was homogeneous. In the proximity of the silicon chamber walls where heat is effectively conducted away they found a large temperature drop. Lin *et al.* [27][28] used a chip with a PCR chamber much like the in the previous presented devices. However instead of using integrated thin film heaters they used a external mounted thermoelectric (TE) device for heating and cooling. The principle of the device is shown in figure 1.3. In this design the entire chip is heated to the target temperature, unlike the chips which have integrated heaters that are thermally isolated from the bulk substrate by placing them on a thin membrane. Due to the larger thermal mass of such a system the reported heating and cooling rates were quite low, only 4°C/s and 2°C/s , respectively. FEM simulations showed that if the temperature at the heater surface was uniform then during steady state conditions there would also be uniform temperature distribution in the PCR chamber identical to the temperature of the heater. The simulations also showed that even during temperature transition the temperature in the chamber an the heater would be virtually identical.

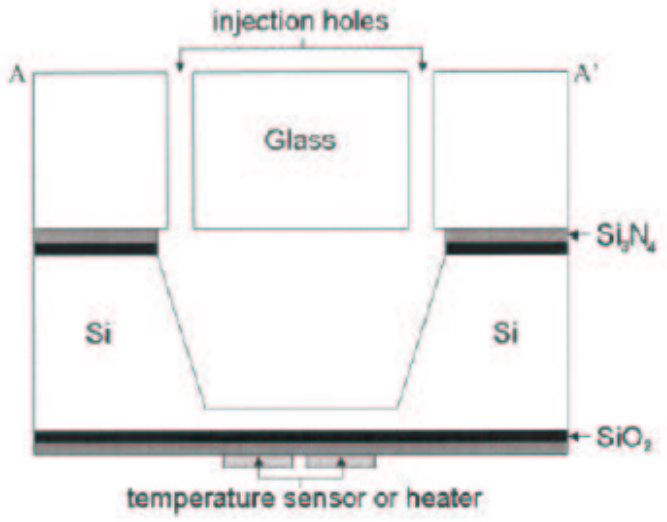

Figure 1.2: *Schematic of a typical silicon based PCR chips. The PCR chamber is etched into the silicon and sealed by bonding of a lid. Heaters for controlling the PCR thermocycling are isolated from the substrate by placing them on a membrane. [24]*

Using transient liquid crystal thermometry of a PCR device similar to the design used by Lin, Chaudhari *et al.* [25] experimentally verified that the temperature distribution in such a design is homogeneous, with the temperature difference in the chamber being less than 1°C, even during temperature ramps of up to 2°C/s.

Bio compatibility is another important issue in the design of PCR chips. Due to the large surface-to-volume ratios in PCR chips surface effects can often inhibit PCR. Schoffner *et al.* [29] made a detailed study on the PCR inhibitory effect of typical surfaces found in silicon micromachined PCR chips, as well as the effect of different surface coatings. They found that surfaces of silicon and silicon nitride (Si_3N_4) exhibited inhibitory effects. The only surface commonly found in silicon micromachined structures that did not inhibit PCR was silicondioxide (SiO_2). However the PCR inhibiting effect of the silicon and nitride surfaces could be removed by treating the surfaces using a silanizing agent, especially if a polymer coating of the surfaces was applied also. Oxide coatings have been used in several of the silicon based PCR chips [23, 27, 30, 31, 24, 32], with polymer coatings [24, 22] and silanization [21] used in others.

1.1.2 Polymer based PCR chips

In recent years polymer based microdevices have increasingly been developed as an alternative to silicon and glass based devices. The main drivers of polymer based systems are the good material compatibility with chemical and biochemical assays and the cost advantage that the relatively inexpensive polymer materials can offer compared

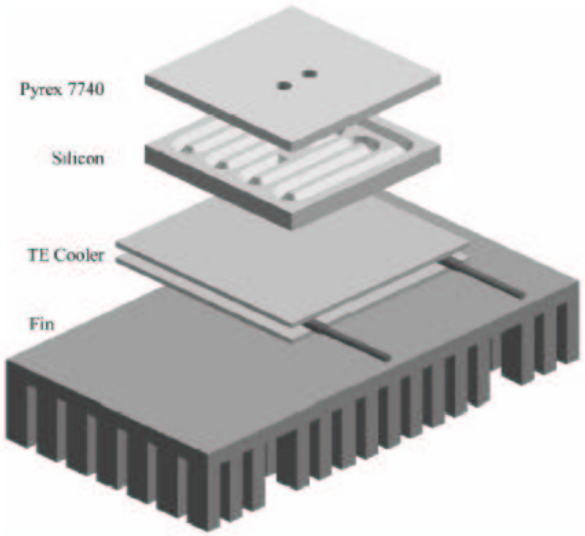

Figure 1.3: *Schematic of silicon based PCR chip with external mounted thermoelectric (TE) device. The chip is mounted on the top side of the TE device and a heatsink is placed on the bottom side. The thermoelctric can be used for both heating and cooling of the chip [27].*

to silicon and glass based solutions. Conventional PCR systems perform the PCR amplification in polypropylene tubes and in the study of Shoffner *et al.* [29] many of the tested polymer surface coatings showed good PCR compatibility.

Only a few polymer based PCR chips have been presented to date. Hong *et al.* [33] have made a PDMS-glass hybrid PCR microchip and Liu *et al.* [34] made a Polycarbonate mico PCR device. In both designs external heating elements in form of peltier thermal electrical devices have been used to control the thermocycling. The presented heating and cooling rates were relatively low, with Hong *et al.* [33] reporting heating and cooling rates of 2-4°C/s and 1-3°C/s, respectively. Liu *et al.* [34] reported slightly higher heating and cooling rates of 8°C/s and 5°C/s, respectively. In both of these polymer based chips no special coating of the PCR chamber surface was necessary to perform the PCR amplification. A completely different external heating method in form of infrared (IR) radiation have been used by Giordano *et al.* [35] in there polyimide PCR chip. They reported identical heating and cooling rates of 10°C/s and that they were able to perform a 15 cycle PCR amplification in less than 240 seconds, the fastest successful amplification reported in literature. IR heating have also been applied to some glass based PCR micro devices [36, 37].

All polymer based PCR chips presented in literature so far have used external elements to control the PCR thermocycling. The PCR chip presented in this thesis is also polymer based, however the chip will have fully integrated thin film heaters and temperature sensor for PCR thermocycling. The polymer chosen in this project is the

epoxy based photoresist SU-8. To the authors knowledge this is the first example of a polymer based PCR chip with fully integrated heaters and temperature sensor to control the PCR thermocycling and also the first example of a PCR chip where the PCR chamber is defined in a photoresist. This simplifies the fabrication process and, as will be shown in this thesis, can alow on chip integration of PCR with a sample pretreatment system and potentially with other functionality.

1.1.3 Flow-through PCR

Most of the PCR chips that have been presented in literature have been of the chamber type like the ones described above. In these systems the sample is stationary and the whole PCR chamber is cycled up and down in temperature. A different approach was presented by Kopp *et al.* [38]. A schematic of the principle is shown in figure 1.4. The sample flows continuously across three different temperature zones at the denaturation, extensions and annealing temperatures of the PCR cycle, respectively. The layout of the flow channel determines the amount of time a sample plug resides in each of the temperature zones. Flow-through chips with integrated heaters to control the temperature of the different zones have been presented by Schneegass *et al.* [39] and Sun *et al.* [40].

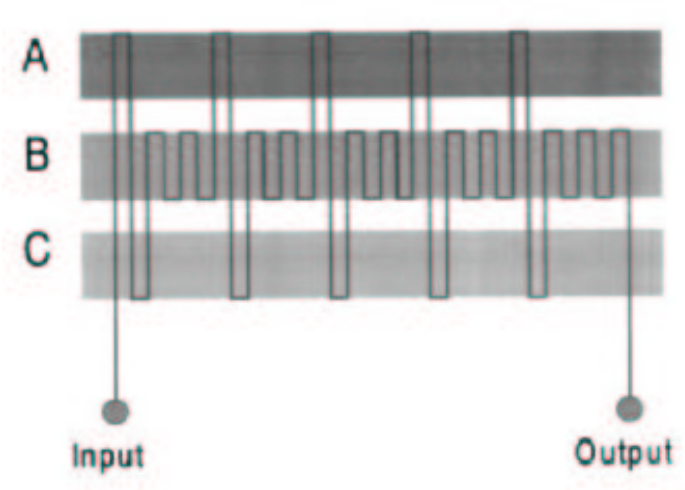

Figure 1.4: *Schematic of a flow-through PCR design. Three temperature zones are kept at denaturation, extension and annealing temperature of the PCR cycle. A flow system passes through the temperature zone defining the PCR cycle [38].*

1.1.4 Integration with other devices

To get the full advantages of a μTAS the PCR chips needs to be integrated with devices for either sample pretreatment or post PCR analysis. In the hybrid approach this is done by connecting separately fabricated devices while the monolithic approach

integrates the devices on one chip. The on chip integration of PCR with other devices for sample pretreatment or post PCR analysis requires process compatibility in the microfabrication process. This often complicates the fabrication procedure and adds limitations to the integrated functionality.

Woolley *et al.* [41] presented a device that integrated PCR with capillary electrophoresis (CE) for post PCR analysis using the hybrid approach in 1996. Waters *et al.* [42, 43] integrated PCR and CE onto a single glass chip. However, no elements to control the PCR thermocycling were included in the design. The thermocycling was performed using commercial thermal cycler equipment. Lagally *et al.* also integrated PCR and CE on a glass chip, initially with external elements for the thermocycling [44], but recently an integrated design using thin film heaters to control the thermocycling has been presented [45]. This device can perform PCR amplification and analysis using only 200 nL sample volume in less than 15 minutes. Another integrated device for DNA amplification and analysis have been presented by Burns *et al.* [46]. They integrated a gel electrophoretic separation system including photodiodes for detection with PCR amplification on chip. Lee *et al.* [47] have recently developed an integrated PCR and electrophoresis system that also includes an integrated optical system for detection. The polymer based PCR chip from Hong *et al.* [33] included a separation channel for CE, while the polymer based PCR chip from Liu *et al.* [34] integrated a hybridization assay. As mention earlier both chips used external elements for the PCR thermocycling in form of a Peltier element and IR heating, respectively. Most of the integration efforts between PCR and other devices presented in literature have focused on coupling PCR with post PCR analysis systems. Wilding *et al.* [30] combined their silicon based PCR chamber with a simple sample pretreatment system in form of a microfilter for cell isolation. Again external elements were used for the thermocycling.

The polymer based PCR chip presented in this thesis will be integrated on chip with a sample pretreatment system that is able to perform several sample preparation steps, while still using fully integrated thin film heaters and temperature sensor to control the PCR thermocycling. To the authors knowledge this is the first device that integrates advanced sample pretreatment with PCR on a micro chip.

1.2 DEP manipulation of cells on microchips

The task of the sample pre-treatment system in this thesis is to prepare the sample for PCR amplification. When working with bioanalytical application the original sample is often in form of whole cells suspended in an aqueous media. Dielectrophoretic (DEP) devices have shown great potential in the manipulation and separation of cells [48] and have therefore been chosen as the technology used in the sample pretreatment system. DEP devices can perform many of the typical sample pretreatment tasks commonly encountered in connection with PCR amplification, like pre-concentration of sample and removal of unwanted components that could inhibit the PCR amplification.

Dielectrophoresis is the motion of cells or particles by electrical polarization effects in inhomogeneous electric fields. The strength of the force acting on the cells increases with the gradient of the electrical field squared. Micro fabricated planar electrodes are very good at producing high field gradients making the technology suitable for microchip applications. Depending on the dielectric properties of the cell, the media and the frequency of the applied field the force can either be towards high field gradient, called positive dielectrophoresis (p-DEP), or towards the region of low field gradient, called negative dielectrophoresis (n-DEP) [48]. The region of high field gradient is always at the electrode edges and this is where cells will be trapped under the influence of p-DEP. The regions of lowest field gradient is either between the electrodes or on top of the electrodes and this is the regions cells moves to under the influence of n-DEP. As the force acting on the cell is proportional to the gradient of the electrical field a cell under the influence of n-DEP is much weaker bound than cells under the influence of p-DEP. Several techniques for separation and manipulation of cells are available by using combinations of DEP force, fluid flow and travelling electrical fields and a vast amount of examples have been presented in literature. Since it is beyond the scope of this thesis to present all of them here only a few examples relevant for the intended use as sample pretreatment system integrated on a PCR chip will be given.

1.2.1 Cell capture

One of the simplest methods where DEP can be used to separate wanted cells from unwanted components or cells is by the cell capture method. In this method the wanted cells are captured by p-DEP at the electrode edges, while unwanted components are removed using liquid flow. This is done by choosing a frequency of the applied electrical field where the wanted cells experience p-DEP and the unwanted components experience n-DEP. Figure 1.5 shows typical electrode structures used in cell capture devices, as well as an example on DEP force dependents on cell type and frequency of the applied electrical field. The separation technique can be reversed by choosing a frequency where the unwanted cells are captured by p-DEP at the electrodes while the wanted cells are collecting in the flow stream.

The cell capture technique has been applied for separation of species in a number of biological samples. Wang *et al.* [50] used it to separate viable from non-viable yeast and bacteria from blood cells. Markx *et al.* [51, 52] also did separations on viable and non-viable yeast as well as on bacteria, while Talary *et al.* [53] separated and enriched stem cells from blood. DEP cell capture has also been used to remove leukaemia cells from blood [54] and to separate cancer cells from blood [55].

1.2.2 Travelling wave dielectrophoresis

A different approach to cell separation and up concentration is used in travelling wave dielectrophoresis (TWD) where the cells can be moved by a travelling electrical field instead of by flow in the liquid. Cell experiencing p-DEP will be stationary in the field as they are immobilized at the electrode edges. Cells under the influence of n-DEP

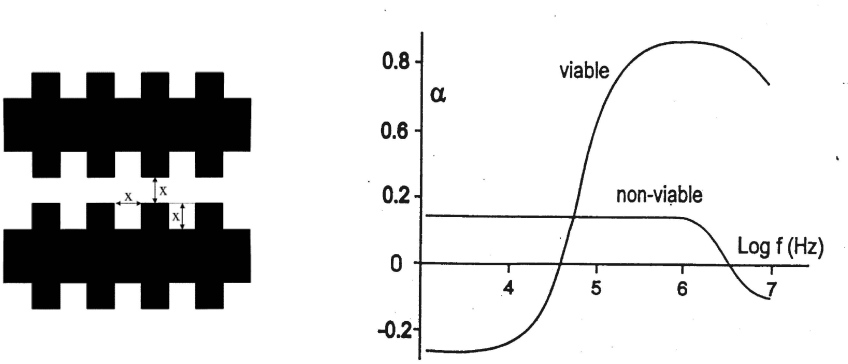

Figure 1.5: *To the left is shown typical castellated electrodes used in DEP cell capture devices. The dimension X of the electrodes is 2-20μm and thus comparable to cell dimensions [49]. To the right is shown a plot of the frequency dependence of the DEP force of viable and non-viable yeast. When the polarizability α is negative the cells are under the influence of n-DEP and will collect between the electrodes, when positive the cells experiences p-DEP and will collect at the electrode edges. By choosing the right frequency the viable cells can be separated from the non-viable [48].*

are however free to move and will do this if the applied travelling electrical field also induces a torque on the cells. Two examples of electrode geometries used to produce travelling electrical fields in planar electrodes are shown in figure 1.6. One is a single electrode layer spiral type structure, the other a two electrode layer track type TWD structure.

Using the spiral type TWD structures Goater *et al.* [56] and Wang *et al.* [58] up concentrated cells by moving them to the center of the spiral structure with the applied travelling electrical field. Talary *et al.* [59] used the track type TWD structures to separate viable and non-viable yeast while Morgan *et al.* [60] separated two different cell types.

Both the cell capture technique and the TWD structures will be considered in this thesis as options for a DEP based sample pretreatment system integrated on chip with PCR. The advantage of the cell capture technique is that single layer electrodes are easier to fabricate than the two layer structures used in the track type TWD, however the fluidic handling when using the capture technique can be more complicated.

1.2.3 Other DEP based techniques

Besides the two techniques described in the previous sections a variety of other DEP based techniques for cell manipulation and separation exist. In DEP based field-flow fractionation DEP induced levitation of cells combined with the parabolic flow profile of laminar flow in microchannels is used to separate species. The principle is shown in figure 1.7. The cells are levitated to a height where the DEP force is countered

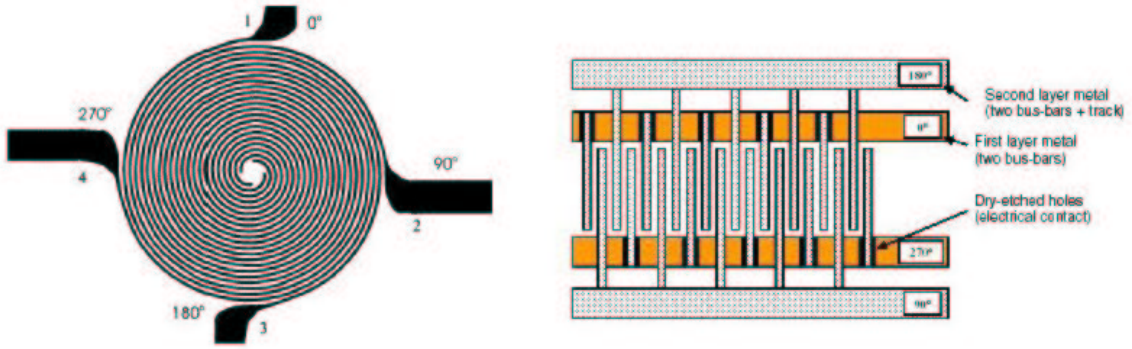

Figure 1.6: *Examples of two designs used for travelling wave dielectrophoresis. The design to the left uses four parallel spirals elements connected to four 90 degrees phase shifted signals and can be implemented using a single electrode layer. Depending on the order of the signal phases there will be a travelling electrical field towards or away from the center of the structure [56]. In the design to the right a two layer electrode structure is used to implement a continuous 90 degrees phase shifted signal down an electrode track [57].*

by gravity. This height is cell dependant and cells will move with different velocity depending on their position in the flow channel and thereby spatially separated.

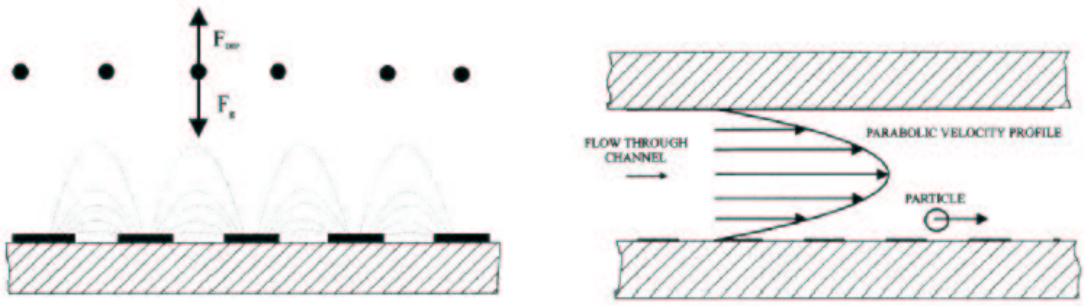

Figure 1.7: *Principle of DEP based field flow fractionation. To the left: Cells are levitated by the DEP force to a height where the force is countered by gravity. The height depend on the cell type. To the right: Due to the parabolic flow profile of laminar flow cells will move with different speed according to there position in the channel. [61]*

Markx *et al.* [61] presented field flow fractionation devices to separate latex beads of different size while Rousselet *et al.* [62] presented a device to separate cells from latex

beads. Gasperis *et al.* [63] combined a TWD structure with field flow fractionation to perform a 2-dimensional separation of cells. Several other DEP based manipulation and separation devices have been presented in literature in form of free flow devices where cells are deflected to different positions using n-DEP [64, 65], three dimensional grid electrode devices [66], dielectrophoretic tweezers [67] and many others.

1.3 Optical detection

Optical detection is probably the most widely used detection scheme in both chemical and bio-analytical analysis. All the analysis systems integrated with PCR chips described earlier uses an optical detection scheme. Optical detection can also be used directly in connection with PCR. By using fluorescent probes real-time monitoring and analysis of the PCR amplification is possible [68, 69] and several commercially available systems exist [70, 71]. Real-time monitoring has also been applied to micro fabricated PCR chips [72, 73, 74, 75, 76]. A number of cell handling devices also incorporates optical detection [77, 78]. Optical detection can thus be used in both the sample pretreatment system as well as for sample analysis in the PCR chip presented in this thesis.

1.3.1 Integrated optics

Most biochemical microdevices that use optical detection rely on bulk optics. Due to alignment requirements and shock stability, packaging of such devices is often difficult and costly. Miniaturization of free space optical elements is also very difficult. Planar optical waveguides monolithically integrated with microfluidic systems may offer a viable solution to these problems. A few systems based on integrated glass waveguides have been presented [79, 80], but they can be difficult and time consuming to realize. An alternative is to use polymer waveguides. Lee *et al.* [47, 81] have used buried SU-8/Spin-on-glass (SOG) waveguides, while McMullin [82] used UV laser writing of optical adhesive spun onto a glass substrate for planar waveguide and microfluidic channel fabrication.

In this thesis SU-8 based planar polymer waveguides have been developed and characterized. Unlike the buried SU-8/SOG waveguides used by Lee *et al.* [47, 81], the waveguides presented here are defined using a single photolithography step giving a simple fabrication process. Furthermore the fabrication process is compatible with the fabrication of the presented SU-8 based PCR chip with integrated DEP sample pretreatment system making future integration possible.

Future integration of planar waveguides would be an important step towards the realization of a fully integrated μTAS. However in the current iteration of the chip, optical access is provided by using an transparent lid to seal the chip and the use of external bulk optical elements.

1.4 Outline of thesis

The aim of this project is to design, fabricate and characterize a PCR chip with an integrated sample pretreatment system. The design will use a SU-8 based PCR chip integrated with a DEP based sample pretreatment. A schematic of the envisioned design is shown in figure 1.8. The SU-8 based PCR chip is fabricated on a glass substrate and is connected on chip with the DEP based sample pre-treatment system using a simple fluidic system. The PCR chip has integrated thin film heaters and a temperature sensor to control the PCR thermocycling. To validate the basic design idea the components are first designed, fabricated and characterized separately. Based on the findings an integrated design is developed. As a step towards a true μTAS, polymer waveguides for integrated optics, compatible with the fabrication techniques used for the PCR chip have also been developed and characterized, but have not yet been integrated with the current design. In this thesis the emphasis will be on the design and fabrication of the components and only simple applications will be described.

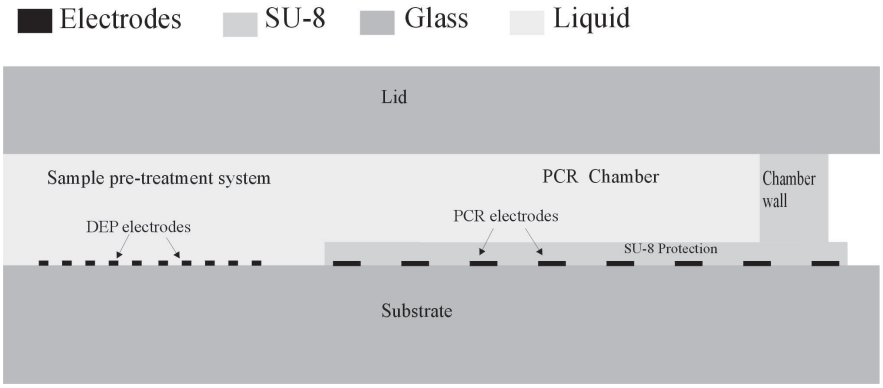

Figure 1.8: *Schematic of envisioned design for integration of PCR with sample pre-treatment. A DEP based sample pre-treatment system is integrated on chip with a SU-8 based PCR chip fabricated on a glass substrate. The chip integrates thin film electrodes to control the PCR thermocycling.*

Outline of chapters

- In chapter two the design and simulation of a SU-8 based PCR chip is presented. Extensive thermal simulation has been used to optimize the design.

- In chapter three the fabrication and packaging of the PCR chip will be described.

- Characterization and validation of the PCR chip design will be described in chapter four. This includes both thermal and bio-analytical characterization.

- Chapter five describes the design, fabrication and characterization of DEP structures for cell manipulation and sample pretreatment

- In chapter six the design of the integrated chip is presented. The design will be based on the findings in the previous chapters.

- The fabrication of the integrated chip is described in chapter seven.

- The integrated chip is characterized in chapter eight.

- Chapter nine deals with the development of polymer waveguides for integrated optics.

- Finally a conclusion of the thesis presenting the most important results will be given in chapter ten

Chapter 2

Design and simulation of PCR chip

In this chapter design and simulation of a microfabricated SU-8 based PCR chip with integrated platinum heaters and a temperature sensor for PCR thermocycling is presented. The basic design is described along with the requirements for the chip. PCR compatibility tests and thermal simulations are then used to validate and optimize the design. Based on this a final PCR chip design is presented.

2.1 Basic design

In this section the design for a PCR thermocycler chip with integrated heaters and temperature sensor is presented. This chapter only deals with the PCR chip design. However, the vision is that the PCR functionality will later be monolithically integrated with a DEP-based sample pretreatment system. Therefore process compatibility and integration issues with such a system have been considered in the development of the design. Besides this there are a range of requirements the PCR chip design needs to fulfill. These are listed below.

- PCR compatibility
- Homogeneous temperature distribution
- High heating and cooling rates
- Low power consumption
- Optical access to PCR chamber
- Ample sample volume for off-chip analysis

The two first requirements are the most important. The PCR chamber needs to be PCR compatible and this is mainly related to the surface properties of the PCR chamber. Some surfaces can for various reasons inhibit PCR amplification. This is especially a problem in microfabricated PCR chips because of the large surface-to-volume ratios in such devices. The second important requirement is homogeneous temperature dis-

tribution. This is important because PCR uses a series of thermally controlled reaction steps where the temperature setting needs to be accurately controlled for optimal performance. High heating and cooling rates are important for fast transitions between the different reaction steps of the PCR thermocycle, but are not essential for the PCR functionality. Neither is the power consumption, but low power consumption makes the design of the power supply easier. Optical access to the PCR chamber makes in situ real-time monitoring using fluorescent probes possible, while ample sample volume is needed for easy external handling of the PCR amplicon. We have decided to use a sample volume of $\sim 20\mu$L.

The basic design idea is shown in figure 2.1. It consist of a $\sim 20\mu$L SU-8 based PCR chamber fabricated on a glass substrate. Thin film platinum heaters and temperature sensors for PCR thermocycling are integrated on chip at the bottom of the PCR chamber. The platinum electrodes are protected from the PCR buffer by a thin layer of SU-8. The chamber is sealed by bonding a lid at the top using a suitable bond layer. The chip is passively cooled by thermal conduction through the substrate to a heat-sink and by natural convection from the lid.

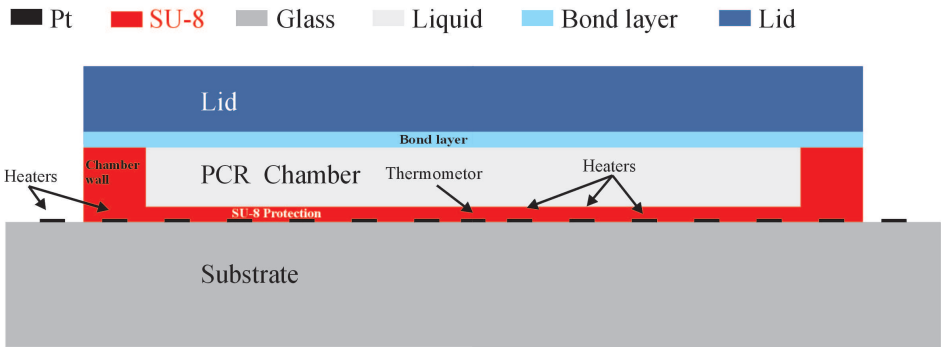

Figure 2.1: *In the figure is shown a schematic of the PCR chip design with a SU-8 based PCR chamber on a glass substrate. The PCR thermocycling is controlled by integrated thin film platinum heaters and thermometer at the bottom of the SU-8 based PCR chamber. The thermometer is placed in the center of the chamber. The platinum electrodes are protected from the PCR buffer by a thin layer of SU-8. The heaters continue beneath and beyond the SU-8 chamber walls to minimize cold wall effects.*

Reasons for making a SU-8 based PCR chip include simple fabrication of fluidic components like flow channels and reaction chambers offered by standard SU-8 processing techniques. This not only helps with the fabrication of the proposed design, it will also help with the envisioned integration of PCR with the DEP-based sample pretreatment system. Furthermore, the surface properties of SU-8 can be easily controlled or altered by plasma treatment or chemical treatment. The PCR compatibility of the proposed design depend on the properties of the SU-8 electrode protection layer, the SU-8 chamber wall, and the property of the bond layer used for the lid. The requirements of the

bond layer is that it has to be PCR-compatible as well as being able to make a tight seal for the lid. If the bond layer for the lid makes an irreversible seal, the fluid interconnects have to be made either through the substrate or the lid. This complicates the fabrication of the chip as well as the packaging. Because the optical access to the PCR chamber is through the lid both the lid and the bond layer needs to be transparent. For transparent lids one can use either glass or polymers. The bonding methods considered for the design are PDMS pressure bond seal and SU-8 to SU-8 bonding. The PDMS bonding is a reversible bond method, while SU-8 to SU-8 bonding generates an irreversible seal.

In the next section the issue of PCR compatibility will be considered, while the following sections will deal with the thermal properties of the PCR chip design. Based on the findings a final design for a PCR chip will be presented.

2.2 PCR compatibility of surfaces

For the envisioned design to be PCR compatible the SU-8 surfaces of the PCR chamber needs to be PCR compatible. If SU-8 to SU-8 bonding is used to bond the lid there will be SU-8 on all surfaces and then PCR compatibility of SU-8 is enough. If a PDMS bond layer is used this must also be PCR compatible. To test if SU-8 and PDMS are PCR compatible a series of PCR amplification experiments were conducted [83]. The surfaces were tested under conditions with surface to PCR buffer volume ratios similar to a typical 20μL PCR chamber. Other surfaces, like Si, SiO_2 and Si_3N_4, which would typically be present in alternative PCR chip designs were also tested. The surfaces were tested in both an untreated and silanized form, using Dichlorodimethylsilane as silanizing agent. The results are summarized in table 2.1. Details about the test can be found in [83].

Table 2.1: *PCR material compatibility table*

	Untreated	Silanized
Si	-	++
Si_3N_4	-	++
SiO_2	+	++
PDMS	++	-
SU-8	-	++

- no signal + small signal ++ good signal

As seen in table 2.1 both silanized SU-8 and untreated PDMS have good PCR compatibility, while untreated SU-8 had poor PCR compatibility. In general it was found that all silanized surfaces tested, with the exception of PDMS, showed good PCR compatibility.

Although untreated SU-8 did not have the good PCR compatibility we had hoped for, the results show that by silanizing the SU-8 surfaces and by using non-treated PDMS, the proposed PCR chamber should be PCR compatible. Thus if the thermal properties of the PCR chip design fulfill its requirements the design should be functional. In the next sections modelling of the thermal performance of the design will be considered.

2.3 Thermal simulations

The thermal performance of different chip designs have been modelled using simple analytical 1D and 3D heat transport models, 1D equivalent circuits models, and 2D and 3D finite element modelling (FEM). The properties of interest include temperature homogeneity, power consumption and heating- and cooling-rates.

The relatively simple 1D and 2D models were used to extract the basic performance of different design configurations. Based on this a final design was chosen that showed good performance with regards to all the thermal properties of interest. The detailed performance of this design was then modelled using more advanced, but also computationally demanding 3D finite element models.

2.3.1 Model assumptions

In order to ease the implementation of the thermal models a number of assumptions have been made. As the PCR chip operates below 100°C radiation losses can be neglected. Only heat transport by conduction and convection needs to be considered. Because passive cooling of the chip is used this leaves thermal conduction and natural convection. In the thermal modelling, the bond layer and the electrode protection layer in the design have been omitted since the effects from these layers have been assumed to be small. This is a valid assumption when these layers are thin compared to the substrate, chamber and lid. This is always the case with respect to the SU-8 protection layer, while it may not always be true with respect to the bond layer. The effect that the packaging of the PCR chips might have on the performance of the chips has also been neglected.

2.3.2 1D analytical model

A simple 1D model of the chip can be made by assuming that the area spanned by the heaters is at a specific target temperature. That is the top of the substrate, which is the bottom of the PCR chamber, is held at a uniform temperature by the heaters. Away from the edges the heat transport is essentially 1D. Heat is transported either by conduction through the substrate to a heat-sink or by conduction through the chamber and lid, with natural convection from the lid to the ambient. The principle of the model is shown in figure 2.2. A target temperature of 94°C, a typical denaturation temperature in the PCR themocycle, has been used, while the ambient temperature

and the temperature of the heat-sink have been chosen to be 22°C. The temperature T_A denotes the temperature at the top of the PCR chamber, while T_B is the temperature at the top of the lid. If the temperature T_A is close to the target temperature, then the temperature distribution in the PCR chamber will be homogeneous, which is one of the requirements we have to the performance of the chip.

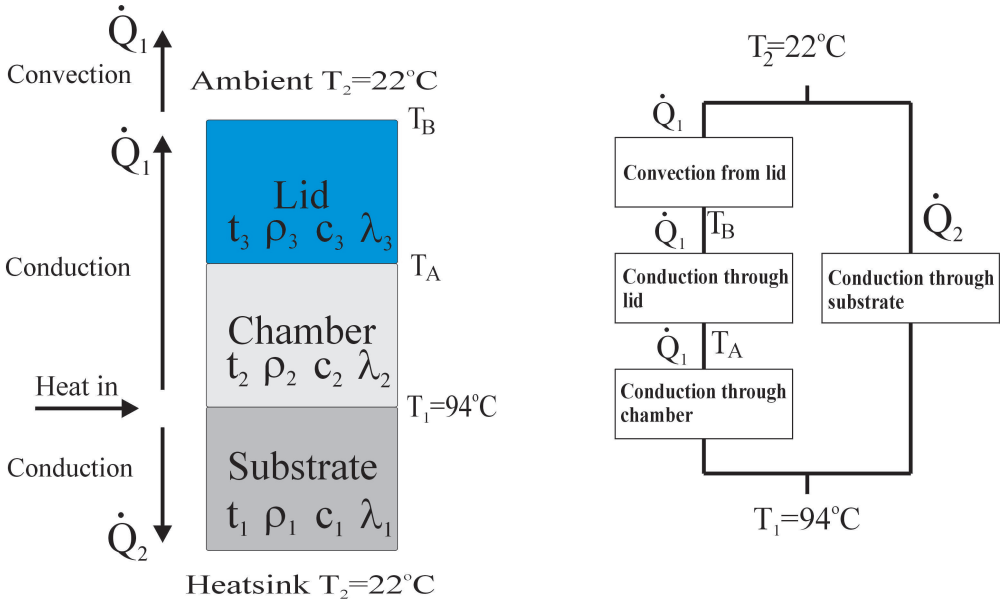

Figure 2.2: *Principle of the 1D heat transport model. The heat generated by the heaters is assumed to provide a uniform temperature at the top of the substrate of 94° C. The generated heat is transported away through two paths. Either by conduction through the substrate to the heatsink, $\dot{Q}_2$, or by conduction through the chamber and lid, and then by convection from the lid to the ambient, $\dot{Q}_1$.*

The two equations needed to describe the heat transport in the analytical 1D model are given in equation 2.3-1 and 2.3-2. Equation 2.3-1 describes the heat transport $\dot{Q}$ by conduction, while equation 2.3-2 describes heat transport by natural convection. To solve the heat transport equations appropriate boundary conditions and a set of material properties are needed. Relevant properties for materials that can be used in the design of our PCR chamber are given in table 2.2.

$$\dot{Q} = \lambda A \frac{\mathrm{d}T}{\mathrm{d}x} \tag{2.3-1}$$

λ is the thermal conductivity of the material, A is the cross sectional area and $\frac{\mathrm{d}T}{\mathrm{d}x}$ is the temperature gradient.

$$\dot{Q} = hA(T_B - T_2) \tag{2.3-2}$$

h is the heat transfer coefficient, A is the cross sectional area and $(T_B - T_2)$ is the temperature difference between the surface temperature, denoted T_B in our model, and the ambient temperature, denoted T_2 in our model, see figure 2.2

Table 2.2: *Material properties table*

	Borosilicate	Fused silica	water	SU-8	PMMA
Thermal conductivity λ $[\frac{W}{m\,K}]$	1.1	1.4	0.6	0.2	0.19
Density ρ $[\frac{Kg}{m^3}]$	2200	2200	1000	1200	1200
Specific heat capacity c $[\frac{J}{kg\,K}]$	700	700	4200	1500	1460

The heat transport equations were solved for typical examples of 1D representations of the possible designs, with substrate thickness in the range from 500-1500μm, chamber height of 400μm and lids with a thickness in the range from 500μm to 750μm. It was found that the vast majority of the heat is lost by conduction through the substrate and to the heatsink. Only a very small fraction, typically less than 0.1%, is lost through the lid, regardless of the lid material is glass or polymer

If we look at the temperature distribution requirement, the simple 1D-model predicts that the temperature T_A at the top of the PCR chamber is in all cases within 1°C of the target temperature. This means that according to the model, the temperature distribution within the PCR chamber will be homogeneous, provided that the temperature is homogeneous at the top of the substrate. Thus fulfilling of the temperature homogeneity requirement for the PCR chamber is a question of finding a heater design that will give homogeneous temperature distribution at the top of the substrate.

Because almost all the heat is lost by conduction through the substrate, the power consumption, P, needed to hold the PCR chamber at a target temperature, depends linearly on the target temperature, T_{Target}, and is inversely proportional to the thickness, $t_{substrate}$, of the substrate, $P \propto \frac{T_{target}-T_{heatsink}}{t_{substrate}}$.

The simple analytical 1D-model is not able to predict transient phenomena like heating and cooling rates. However, a modified version of the model using equivalent circuits can be used for transient analysis. This model is described in the next section.

2.3.3 SPICE implementation of 1D-model

The transient heat transport properties needed to asses heating and cooling rates of different designs, can be modelled by implementing an electrical equivalent circuit representation of the 1D heat transport model, and then use SPICE or similar nonlinear network analysis programs to extract static and dynamic information from the model.

From the continuity of heat one gets that the general heat-flow equation is given by equation 2.3-3.

$$\rho c \frac{\partial T}{\partial t} - \lambda \nabla^2 T = S(t) \tag{2.3-3}$$

ρ is the density, c is the specific heat capacity and λ the thermal conductivity of the material. S(t) the heat generated per unit volume, e.g. by a resistive heater. The relevant material properties for materials used in the design of our PCR chamber are given in table 2.2.

The linear partial differential equation 2.3-3 is similar to the differential equation for electrical current flow in an RC-network. Thus the general heat-flow equation can be represented by a simple RC-electrical network analogy. A schematic of the electrical circuit representation of the 1D heat transfer model is shown in figure 2.3, along with the transformation used to get from the physical domain to the equivalent electrical representation. Note that t_i in figure 2.3 represents thicknesses and not time. To increase accuracy the substrate and the chamber was subdivided into 10 regions while the lid was subdivided into 5 regions in the actual implemented SPICE model. This gives a better representation when there is a non-linear temperature distribution, as is the case during transient modelling.

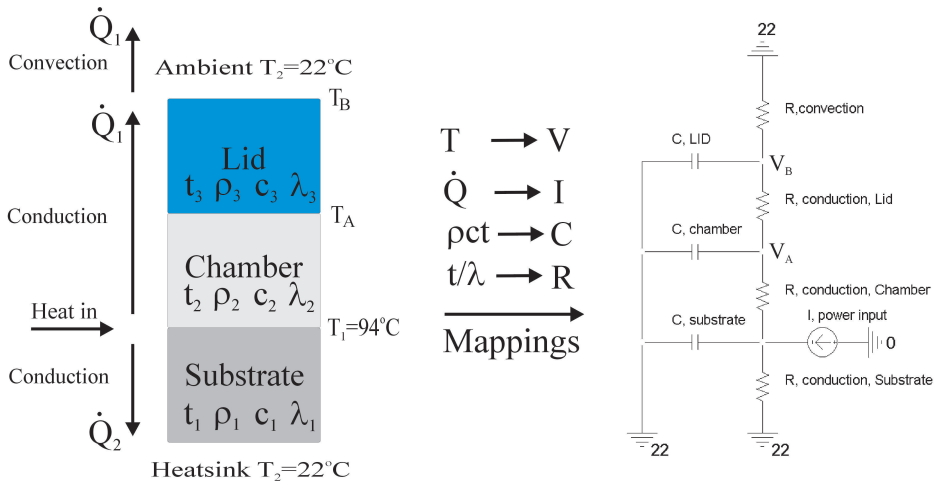

Figure 2.3: *In the left of the figure the physical representation of the 1D heat transport model is shown. The heat generated at the top of the substrate by the heaters is transported away, either by conduction through the chamber and lid, and then by convection from the lid to the ambient, $\dot{Q}_1$, or by conduction through the substrate and to the heat-sink, $\dot{Q}_2$. To the left the equivalent electrical circuit of the 1D heat transport model is shown. The transformation between the physical domain and the electrical domain is shown in the center of the figure.*

The 1D SPICE model can simulate all the steady state properties, like temperature distribution and power usage at specific target temperatures, like the simple analytical

model in the previous section, but also transient responses like heating and cooling rates. The SPICE model is computational efficient, requirering only few seconds to do transient analysis, making analysis of several different designs possible in a very short time. The model is still a 1D model, and thus not able to help in the design of a heater configuration that will give homogeneous temperature distribution at the top of the substrate. For such analysis FEM is required. However, the SPICE model can be used to validate the findings of the more advanced FEM models.

2.3.4 2D ANSYS FEM modelling of heater design

The conclusion drawn from the simple analytical 1D model is that if the heaters can be designed to provide a uniform temperature at the top of the substrate then the temperature distribution in the rest of the chamber will be homogeneous, at least away from the edge of the area spanned by the heater. In this section different heater designs will be investigated, to find a suitable heater configuration that provides a uniform temperature distribution. To find a heater configuration that can achieve this, 2D ANSYS FEM simulations have been used.

A schematic of a typical model that has been implemented in ANSYS is shown in figure 2.4. The model consist of a substrate with a number of heaters, a chamber, chamber wall and a lid. At the bottom of the substrate a heat-sink is connected, while convection loading has been used as a boundary condition on the top of the lid. To reduce the computing requirements, the symmetry at the center of the chamber has been used so only half of the design has to be modelled. All the regions of the design have been implemented to scale in the model, except for the thickness of the heaters, which in the model are assumed to be to 2μm thick, which is approximately a order of magnitude thicker than typical thin film platinum heaters. This was done to avoid regions with extremely large aspect ratios, which are difficult to handle for FEM programs due to inferior mesh quality in such regions. The heating action was modelled by a constant power generation pr. unit area in the heaters. As with the 1D models, the electrode protection layer and the bond layer has been omitted from the model.

A variety of heater designs with different heater spacing and width were modelled using a PCR chamber with an area of 6800μm x 6800μm and a height of 400μm. The camber size was chosen because it represents a chamber volume of the desired 20μL, with a chamber height that can be fabricated using standard SU-8 processing. The models had a 400μm wide SU-8 chamber wall and used 500-750μm glass lids. We know from the analytical 1D model that the steady state properties like temperature homogeneity and power usage only has little dependence on the chamber and lid properties, so the actual choice of chamber and lid configuration will only have negligible influence on the task of finding a proper heater design. The heater designs were tested using substrates with a thickness ranging from 500μm to 1500μm.

The simulations showed that in the entire range of the substrate thicknesses, a heater width of 20-40μm with a heater spacing of 100μm was able to produce a reasonable

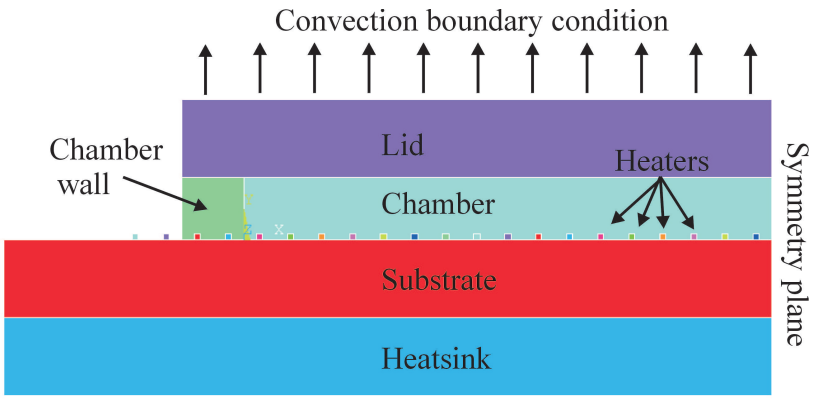

Figure 2.4: *Schematic of a 2D ANSYS model. The model includes heatsink, substrate, chamber and chamber wall and a lid with a convection boundary condition on top. All structures of a design have been implemented to scale in the model, except for the heaters that have been made thicker to avoid extreme aspect ratio structures as these are difficult to handle for FEM programs due to inferior mesh quality in such regions. In this figure the size of the heaters have been increased further for visualization purposes.*

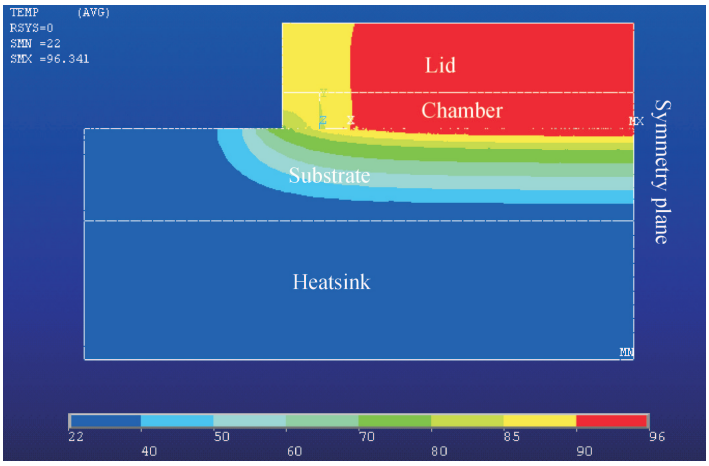

Figure 2.5: *Simulation of temperature distribution in a PCR chip design with 100 μm heater spacing and heaters that extend 700 μm beyond the inner edge of the chamber wall. The temperature distribution in the chamber is homogeneous, within $\pm 2°C$ of the target temperature $94°C$ except near the edge of the chamber where there is a small temperature drop.*

uniform temperature at the top of the substrate away from the edge of the heater array. Near the edge of the heater array there was a quite significant temperature drop. To minimize the effect of this temperature drop on the temperature distribution in the PCR chamber the heaters were designed to continue beneath and beyond the PCR chamber wall, as shown in figure 2.1 and 2.4. Figure 2.5 show a simulation of the

temperature distribution in a chip design with 100μm heater spacing and with heaters that extend 700μm beyond the inside of the PCR chamber wall, giving a total of 82 resistors with a length of 8200μm for the 20μL chamber. The temperature distribution in the PCR chamber is almost homogeneous, with the majority of the chamber within $\pm$2°C of the target temperature 94°C. There is however, still a small temperature drop at the edge of the chamber and this is why the temperature distribution is not as homogeneous as the 1D models predict. The inhomogeneity has been judged to be negligible and we have chosen the above heater configuration for our PCR design.

2.3.5 Optimization of the design

The very important requirement for temperature homogeneity has been satisfied by choosing a proper heater design. Now optimization of the design with respect to power consumption and heating and cooling rates is left. Heating and cooling rates can be modelled using transient simulations with the 1D SPICE and 2D ANSYS models presented in the previous sections, while the power consumption can be modelled using steady state analysis of the 2D ANSYS model and by the simple analytical 1D model. The achievable heating rate is basically more dependent on the power supply and the control system used than the actual chip design. However, because passive cooling is used the cooling rate is very dependent on the design, especially the substrate thickness. Therefore the design optimization has focused on finding a chip design with a thickness of the substrate that provides fast cooling rates, but also a reasonable power consumption. The 2D ANSYS simulations have been made using the heater configuration and the PCR chamber used for the simulations in the previous section. The lid has been assumed to be a 750μm glass lid. A heated area of 8200μm x 8200μm, which is identical to the area spanned by the heaters in the FEM models, has been assumed in the 1D model, so that the power consumption can be compared. In all cases the target temperature of the PCR chamber is 94°C. Substrate thicknesses from 500μm to 1500μm have been investigated. The glass substrate is assumed to be borosilicate type glass, like Pyrex or Borofloat.

In figure 2.6 the simulated power consumption as a function of the substrate thickness is shown for both the 2D ANSYS model and the simple analytical 1D model. The 2D ANSYS model agrees well with the 1D model and the expected approximate inverse proportionability of the power consumption with the substrate thickness is found, with power consumption varying from approximately 10W down to just under 4W for substrate thickness in the range from 500μm to 1500μm. It is expected that when the substrate thickness increases there will be an increase in edge effects for the 2D model leading to increased power consumption. This is also found as the power consumption of the 2D ANSYS model decreases at a slower rate with the substrate thickness than the 1D-model. This effect will be discussed in further detail in section 2.3.6.

In figure 2.7 2D ANSYS simulation and 1D SPICE simulation of the cooling rate dependence on substrate thickness is shown. The cooling rate is in this case defined as the average cooling rate between 90°C and 80°C and it has been modelled for two

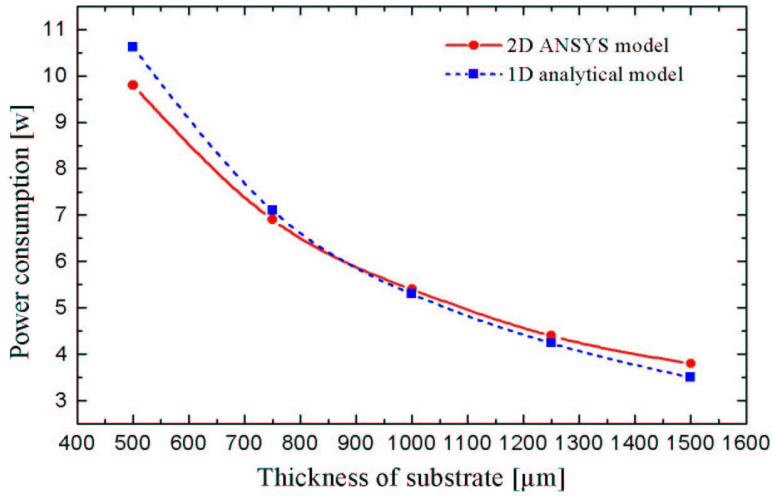

Figure 2.6: *Simulated power consumption as a function of substrate thickness for both 2D ANSYS and 1D analytical model. The 2D ANSYS model predicts approximately the same inverse proportionability of power consumption with substrate thickness as the analytical 1D model.*

positions in the PCR chamber. One position is the top center of the substrate, the position of the thermometer in the design, which is expected to be the position with the fastest cooling rate in the chamber. The second position is at the top center of the PCR chamber, which is expected to be the position with the slowest cooling rate in the chamber. This thus gives the upper and lower bound of temperature transitions in the PCR chamber. As seen in the figure the cooling rate at the top of the chamber is not only lower than at the substrate, it also has weaker dependency on substrate thickness. Both the 2D ANSYS FEM model and the 1D SPICE models agree that the cooling rate at the top of the chamber varies approximately a factor two for the given range of substrate thickness, from approximately 20°C/s with a 500μm substrate down to approximately 10°C/s for the 1500μm substrate. The 1D SPICE model predicts a slightly larger cooling rate than the 2D ANSYS FEM model. Both models also agree on the cooling rate at the top of the substrate being not only larger than at the top of the chamber but also having a stronger dependence on the substrate thickness. With substrate thickness in the range from 1000μm to 1500μm a cooling rate in the range from approximately 40°C/s down to approximately 20°C/s is found, again with the SPICE model predicting slightly higher cooling rates than the ANSYS model. But with a substrate thickness below 1000μm the SPICE model starts to predict a significantly higher cooling rate than the ANSYS model. The reason for the discrepancy between the two models is believed to be that the time stepping in the transient 2D ANSYS FEM model simply can not resolve the extremely fast thermal transition taking place in this region. Automatic time stepping is used in the ANSYS model, but it seem as

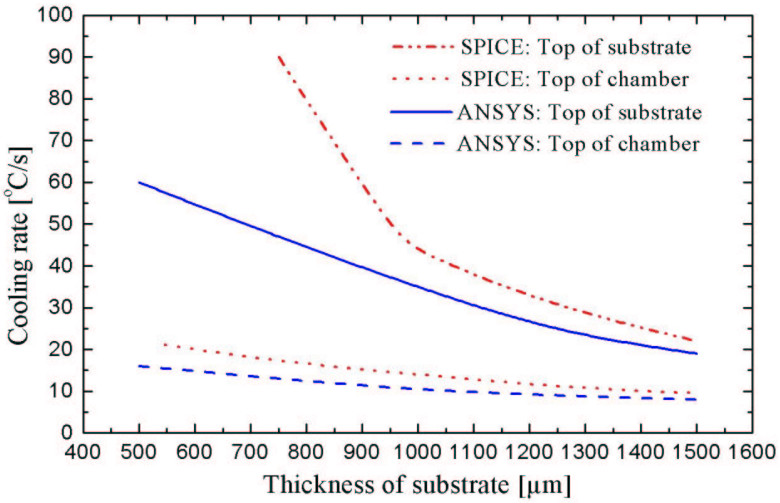

Figure 2.7: *Simulated cooling rate using ANSYS and SPICE for two positions in the PCR chamber as a function of substrate thickness. One position is at the top center of the substrate, the position of the thermometer in the design, while the other position is at the top center of the chamber. There is good agreement between the two models except for the substrate cooling rate when the substrate thickness is below 1000µm, where there is a large difference in the predicted cooling rate. The reason for this discrepancy is that the time stepping in the transient ANSYS FEM model simply can not resolve the extremely fast thermal transition that occur in this region.*

if the solution is not fully converged between the time steps. So while a FEM model is more advanced and can give more information than the simple 1D SPICE model, care must be taken to ensure that the solution is valid.

Figure 2.8 shows a graph of the cooling rate at the top of the chamber and at the top of the substrate divided by the power consumption, as a function of the substrate thickness. The values are taken from the 1D SPICE model. Factoring in both power consumption and cooling rates there is no obvious optimal substrate thickness for the design. However, a substrate thickness of 1000μm presents a good compromise between power consumption and cooling rate, both at the top of the substrate and at the top of the chamber. Thus in the final design of the PCR chip, the chamber and heater design presented in section 2.3.4, is implemented on a 1000μm glass substrate.

2.3.6 3D analytical power consumption model

In this section the dependency of the power consumption on substrate thickness will be investigated, using a simple 3D analytical approximation of the heat transport. In section 2.3.5 it was found that the power consumption of the 2D ANSYS model

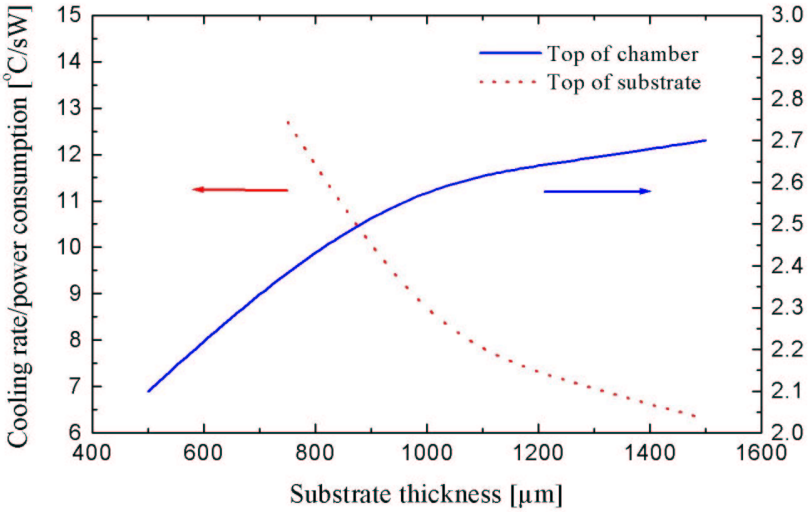

Figure 2.8: *Graph of the cooling rate divided by power consumption as a function of the substrate thickness*

decreases at a slower rate with the substrate thickness than the analytical 1D-model. When heatloss through the lid is neglected the, 1D model predicts that the power consumption P is inversely proportional to the substrate thickness, $P \propto \frac{T_{target}-T_{heatsink}}{t_{substrate}}$. The slower decrease in power consumption of the 2D ANSYS model was attributed to increased heat loss at the edges of the heater array with increasing substrate thickness. To investigate this further a simple 3D model is used.

Figure 2.9 shows a schematic of a simple 3D heat transport model of the PCR chip. The PCR chip is modelled by a hollow hemisphere of inner radius R_1 and outer radius R_2. The area of the inner surface A_1 correspond to the heated area of the PCR chip and this determines the inner radius R_1 of the hemisphere. This area is assumed to be at the target temperature T_1. The difference between the inner and outer radius, R_2-R_1, correspond to the substrate thickness t, and determines the outer radius R_2=R_1+t of the hemisphere. The outer surface of the hemisphere is assumed to be at the temperature of the heatsink T_2. Only heat transport through the substrate is included in the model.

The heat transport through the hemisphere is described by equation 2.3-4.

$$\dot{Q}(R) = -\lambda A(R)\frac{\mathrm{d}T}{\mathrm{d}R} \tag{2.3-4}$$

λ is the thermal conductivity of the material, A(R) is the cross sectional area at radius R and $\frac{\mathrm{d}T}{\mathrm{d}R}$ is the temperature gradient at radius R.

In steady state the heatloss trough the area A(R) will be constant and equation 2.3-4 can be solved by separating the variables and integrating over the boundaries as shown in equation 2.3-5

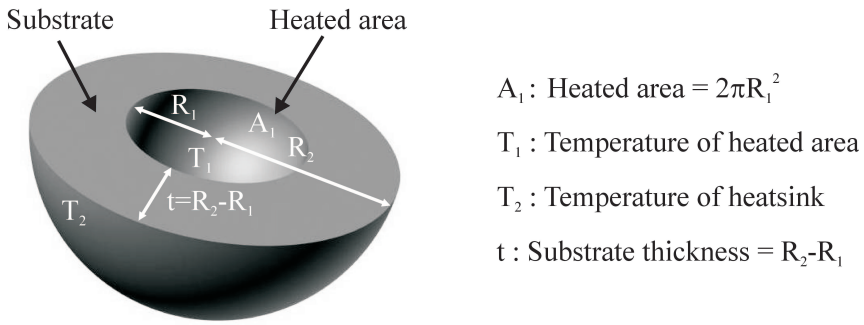

Figure 2.9: *Schematic of 3D analytical heat transport model. The PCR chip is modelled by a hollow hemisphere. The heated area of the PCR chip corresponds to the inner surface of the hemisphere A_1. This area is assumed to be at the target temperature T_1 of the PCR chip. The difference between the inner and outer radius, R_2-R_1, correspond to the substrate thickness t. The outer surface A_2 of the hemisphere is held at the temperature of the heatsink t_2.*

$$-\dot{Q}\lambda \int_{R=R_1}^{R=R_2} \frac{dR}{A(R)} = -\dot{Q}\lambda \int_{R=R_1}^{R=R_1+t} \frac{dR}{2\pi R^2} = \int_{T=T_1}^{T=T_2} dT \tag{2.3-5}$$

By simple integration and some rearranging one gets that the heatloss P through the hemisphere is given by equation 2.3-6.

$$P = \dot{Q} = 2\pi\lambda(T_1 - T_2)R_1\left(1 + \frac{R_1}{t}\right) \tag{2.3-6}$$

From equation 2.3-6 it can be seen that according to the simple hemispherical 3D heat transport model, even as the substrate thickness tend to infinity, there is a minimum power consumption of $P_{min} = 2\pi\lambda(T_1 - T_2)R_1$ needed to maintain the target temperature in the PCR chamber. For a PCR chip with a 8200μmx8200μm heated area (R_1 ~3.27mm) using a borosilicate substrate ($\lambda = 1.1W/m\ K$) and a temperature difference between chip and heatsink of $\Delta T = 72°C$ one gets a minimum power consumption P_{min}=1.64W.

Figure 2.10 shows a plot of the predicted power consumption for both the 1D and 3D analytical models as a function of the substrate thickness. The predicted power consumption of the 3D model is always higher than the 1D model. The power consumption of the 1D model tends to zero for thick substrates whereas the power consumption of the 3D model tends to a finite value.

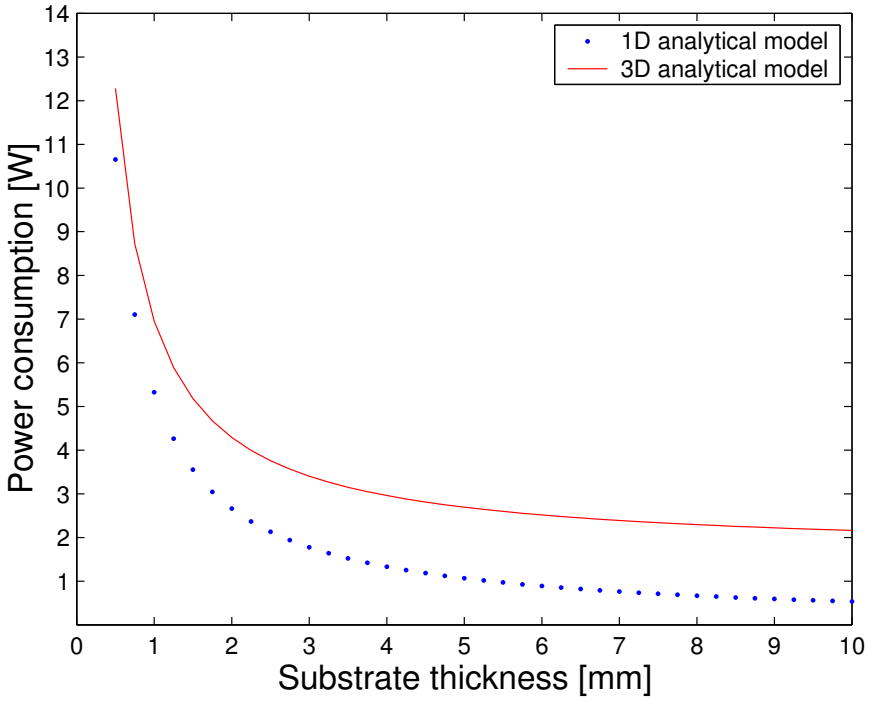

Figure 2.10: *Predicted power consumption as function of substrate thickness for both the 1D and 3D analytical models. The predicted power consumption of the 3D model is always higher than the 1D model, and while the power consumption in the 1D model tends to zero for thick substrates, the power consumption in the 3D model tends to a finite value.*

The simple 3D hemispherical heat transport model always overestimates the power consumption (over estimates the edge effect), whereas the 1D model always underestimates the power consumption (no edge effect included). The errors depend on the size of the heated area compared to the thickness of the substrate. For the final PCR design with a substrate thickness of 1000μm and a heated area of 8200μmx8200μm, the 1D analytical model predicts a power consumption of $\sim$ 5.3W, while the 3D analytical model predicts a power consumption of $\sim$7W. According to the 2D ANSYS FEM simulation the power consumption with a 1000μm thick substrate is $\sim$ 5.5W. Thus for the chosen design the 1D model is pretty accurate.

2.3.7 3D FEM models

To extract detailed information about the expected performance of the chosen design 3D FEM simulations have been used in addition to the 2D and 1D models presented in the previous sections. 3D FEM models in both ANSYS and CFD-ACE were used. Figure 2.11 shows the model implemented in CFD-ACE. As with the 2D FEM models, the heaters were not implemented to scale due to the meshing requirements and the electrode protection layer and the bond layer have been omitted. The 3D CFD-ACE models were build using the CFD-ACE micromesh model generator while the

3D ANSYS models were build manually. The 3D ANSYS model is similar to the 3D CFD-ACE model. A convection boundary condition has been applied to the lid. To model the heat-sink an iso-thermal boundary condition was applied to the bottom of the substrate.

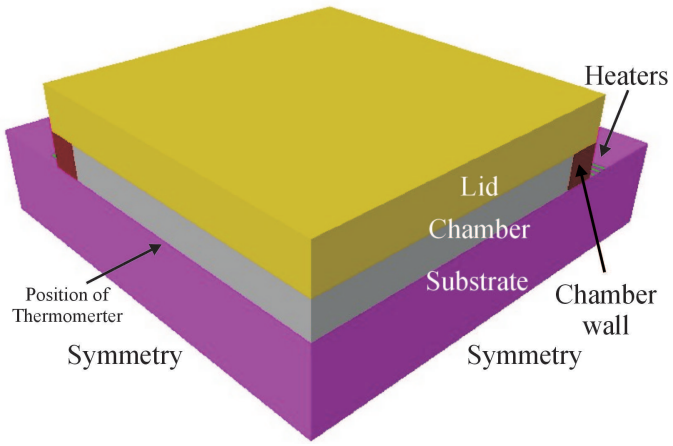

Figure 2.11: *3D CFD-ACE model of PCR chip build using the Micromesh model generator. The model has been implemented to scale, except for the heaters, which for meshing purposes have been modelled as being 2 μm high. 2-fold symmetry has been applied to the model to reduce computing requirements. The position of the thermometer in the model is on the top of the substrate along the left symmetry plane of the model.*

3D FEM simulations are very computationally requiring, especially with transient simulation. Due to software and hardware limitations of the ANSYS simulation setup, only steady state calculations of the final design were performed with the 3D ANSYS FEM model. Both transient and steady state simulations were performed using the CFD-ACE model. The results of the simulations are presented in section 2.5

2.4 Final PCR chip design

Based on the PCR compatibility tests and the thermal simulations presented in the previous section a final design of the PCR chip has been developed that is believed to fulfill the desired requirements. A schematic of the design is shown in figure 2.12. Two slightly different versions of the design have been implemented, version 1 and version 2. Version 2 was developed after it was discovered that the heater configuration in the original implementation, version 1, had a negative impact on the temperature control of the PCR chip. Besides the difference in heater configuration the designs are identical. In both versions a 1000μm boron silicate glass substrate is used, with the approximately 20μL SU-8 based PCR chamber on top. The PCR chamber is 400μm high and has an area of 6800μm x 6800μm. The SU-8 PCR chamber wall has a width

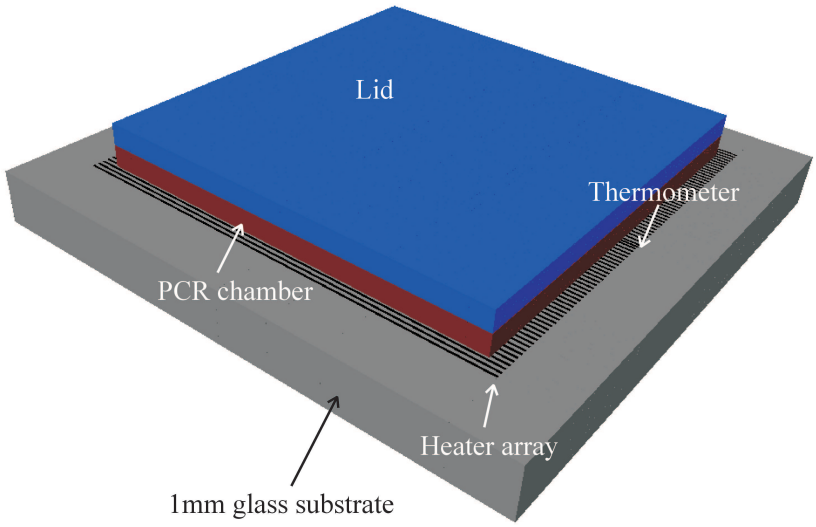

Figure 2.12: *Schematic of final PCR chip design. A 20μL PCR chamber is fabricated on a 1mm boron silicate glass substrate. A resistive thermometer is placed in the center of the PCR chamber with heater arrays for the PCR thermocycling positioned on each side. The heater spacing in the arrays are 100μm and the heaters extend beyond the chamber walls to minimize cold wall effect. The lid can be either a polymer lid or a glass lid and is bonded to the PCR chamber using a suitable bond layer.*

of 400μm. The heater structure consist of a total of 82 heaters in two heater arrays with 41 heaters with a width of 20μm and a length of 8200μm in each of the arrays. The spacing between heaters in an array is 100μm. The two heater arrays are placed symmetrically on each side of a resistive thermometer that is positioned in the bottom center of the PCR chamber, see figure 2.12. The resistive thermometer has a width of 20μm and a length of 7000μm and is connected using 4-terminal connections. In the first version of the design that was implemented (version 1) the heater arrays are placed in such a way that at the position of the thermometer the heater spacing is doubled to 200μm. The implications this has on the temperature control of the devices were discovered after fabrication of the chips and a final version, version 2, of the design was then made. In version 2 the heater arrays are positioned so the heater spacing at the position of the thermometer is 100μm as in the rest of the PCR chamber. The effect of the two different heater configurations will be described in section 2.5.3. The heaters and the thermometer are protected from PCR buffer with a 5μm SU-8 layer. The lid can be either a polymer or a glass lid and can be bonded with either a reversible PDMS bond or an irreversible SU-8 to SU-8 bond. Due to simpler fabrication process and packaging of chips with PDMS bonded lids, almost all of the fabricated devices have been of this type. Only a few test chips with SU-8 bonded lids have been produced.

Fabrication and characterization of the chips will be presented in later chapters. In the next section detailed thermal modelling of the final chip design will be presented.

2.5 Simulation of final design

In this section the expected performance of the PCR chip has been investigated using the 1D,2D and 3D models presented in the previous sections. Power consumption, temperature homogeneity and cooling rates have been simulated and the results of the different models compared. The simulations shown in the next sections are all from version 2 of the design, except in section 2.5.3 where simulations from version 1 have been included to show the implication of the different heater configurations.

2.5.1 Power consumption

Table 2.3 shows the predicted power consumption found by the different models, at a typical denaturation temperature of 94°C.

Table 2.3: *Simulated power consumption for PCR chip at 94°C*

Simulation model	1D	2D ANSYS	3D ANSYS	3D CFD-ACE
Power consumption @ 94°C [W]	5.3	5.5	5.7	5.7

The 1D models predict a power consumption of 5.3W, while the 2D ANSYS FEM model predicts a power consumption of 5.5W. Both the 3D ANSYS model and the 3D CFD-ACE model predicts a power consumption of 5.7W. The increase in power consumption with increasing dimensionality of the model can be attributed to inclusion of extra heat loss from the edges of the PCR chamber.

2.5.2 Temperature homogeneity

A 2D ANSYS simulation of the temperature distribution of in the final chip design was presented in section 2.3.5 on page 24. This showed that the expected temperature distribution in the chamber is almost homogeneous except for a small temperature drop near the edge of the chamber. In figure 2.13 the temperature distribution predicted by the 3D CFD-ACE model is shown. Again a homogeneous temperature distribution is predicted with a small temperature drop near the edges. The view of the temperature distribution at the right symmetry plane in figure 2.13 corresponds to the region modelled by the 2D ANSYS model shown in figure 2.5 on page 24. The simulated temperature distribution in this region by the two models are both qualitatively and quantitatively similar. The temperature distribution predicted by the 3D ANSYS model is almost identical to the 3D CFD-ACE model.

To get a better view of the temperature distribution in the PCR chamber, view planes through the model can be used. In figure 2.14 two view planes through the PCR chamber are shown. To the left the cut is made at a position just above the heaters in the PCR chamber, while the cut to the right is made at the top of the PCR chamber at the position of the lid. It is seen that the effect of the temperature drop is bigger

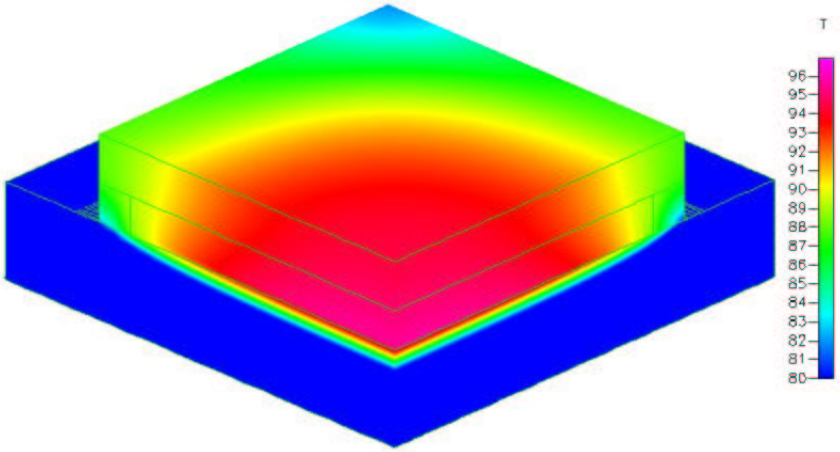

Figure 2.13: *3D CFD-ACE simulation of temperature distribution for the final PCR chip design using a target temperature of 94°. The temperature distribution is homogeneous except for a small temperature near the edges of the chamber.*

in the corners of the chamber where two edges meet and that the region of lower temperature extends further into the chamber at the top of the chamber compared to at the bottom. The temperature distribution in the PCR chamber predicted by the 3D CFD-ACE model is thus not as homogeneous as expected from the 2D ANSYS model. However the current design should still fulfill the requirements for PCR. Data from the modelling predicts that the average temperature in the PCR chamber is approximately 92°C, with more than 3/4 of the chamber at a temperature above 90°C.

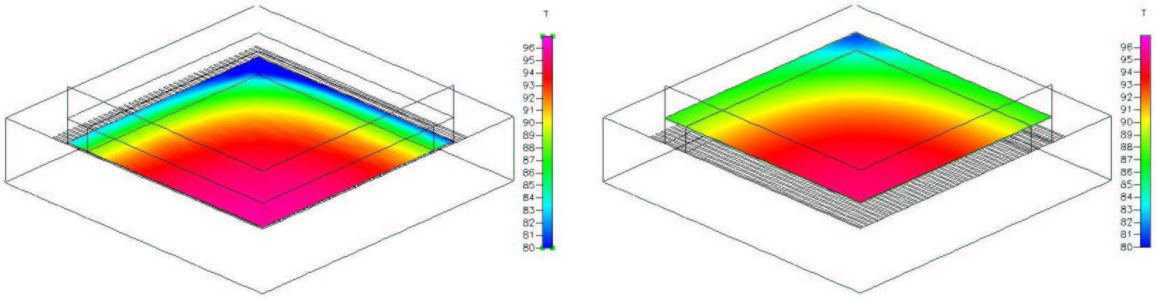

Figure 2.14: *Two z-cut view planes from the 3D cfd-ace temperature distribution simulation. To the left the cut is made just above the heaters at the bottom of the chamber, to the right the cut is made at the top of the chamber. The effect of the temperature drop near edges increases in corner regions of the chamber.*

All models thus indicate that the temperature distribution in the PCR chamber should fulfill the homogeneity requirement, although the performance of the design could be improved by extending the heaters further out from the chamber wall to reduce the temperature drop at the corners and edges.

2.5.3 Temperature distribution at thermometer

It is not enough that the temperature distribution in the majority of the chamber is homogeneous, it is also important that the temperature setting is controlled correctly. The resistive thermometer used in the design extend all the way to the edge of the PCR chamber and is thus also subjected to the temperature drop at the edge of the chamber. Further more, in the first implementation of the design, refereed to as version 1, the temperature sensor acted like a "missing" heater resulting in a 200μm heater spacing in the center of the chamber. In the final implementation of the design, version 2, the temperature sensor was embedded between the heater arrays retaining the 100μm heater spacing at the center of the chamber. To see how these aspects influence the temperature control, the temperature distribution at the position of the thermometer was simulated using the 3D CFD-ACE model.

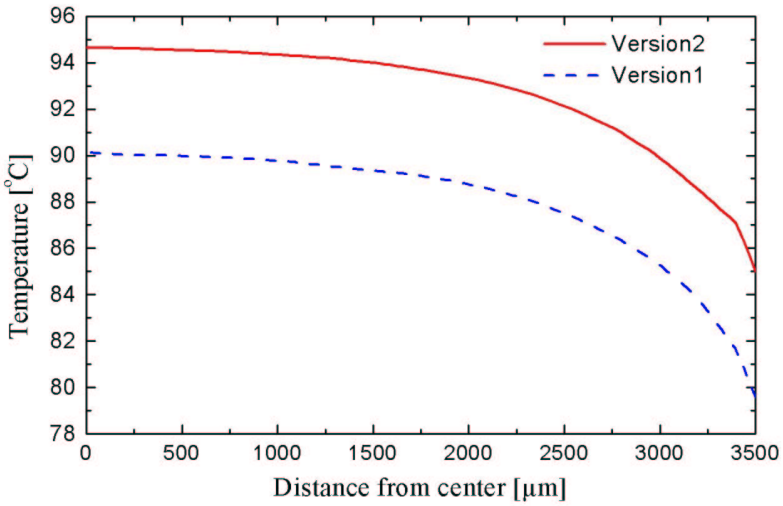

Figure 2.15: *Simulation of the temperature distribution along the thermometer from the center towards the edge of the chamber for two implementations of the design, an old design and the final design. The target temperature in the PCR chamber was 94°. In both designs the temperature drop near the edge is observed, but the temperature in the old design is approximately 4-5° lower than in the final design due to differences in the position of the heater array around the thermometer.*

In figure 2.15 the simulated temperature distribution from the center of the thermometer and towards the edge is shown for the two implementations of the design. The target temperature in the chamber is 94°C. In both cases the temperature drop near the edge is clearly present. In the final design the temperature along most of the thermometer is near the target temperature and the average temperature is in this case just below 93°C and thus only approximately 1 degree different from the target temperature. However in the old implementation of the design due to the 200μm heater

spacing at the thermometer the temperature is approximately 5°C lower, resulting in an average temperature that is 88°C and thus 6°C lower than the target temperature. In the old design, version 1, one has to include this offset between the temperature at the thermometer and the temperature in the majority of the PCR chamber while in the final design, version 2, the temperature reading corresponds well with the actual temperature in the chamber.

2.5.4 Cooling rates

During the PCR thermocycle there is a cooling step were the PCR chamber is cooled from the denaturation temperature, typically around 94°C, to the annealing temperature, which normally is 60°C or lower. Figure 2.16 shows 1D SPICE, 2D ANSYS and 3D CFD-ACE simulations of this cooling step at the position of the thermometer in the PCR chamber. The 1D SPICE and 3D CFD-ACE models have a 500μm thick glass lid while the 2D ANSYS model is with a 750μm thick glass lid to estimate the effect of lid configuration on the cooling rates. The total thermal mass in the 2D ANSYS model is thus higher than in the two other models and lower cooling rates is expected.

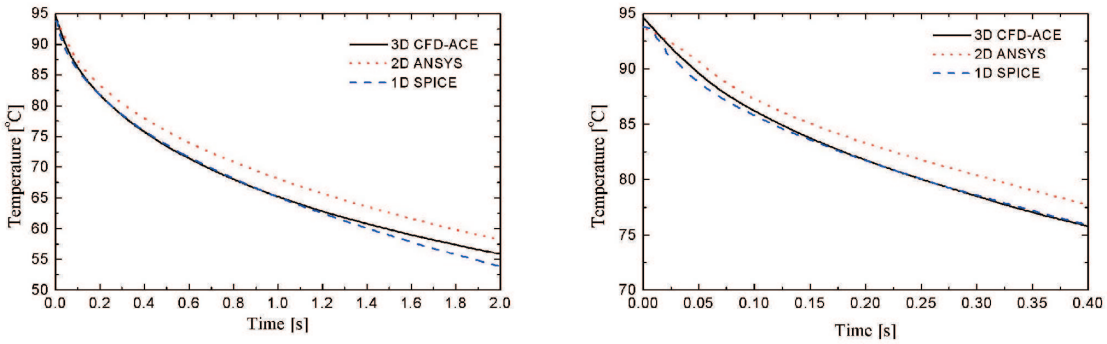

Figure 2.16: *1D SPICE, 2D ANSYS and 3D CFD-ACE simulations of the temperature drop from 94°C when the power to the heaters are turned off at time t=0. To the left the first 2 seconds of cooling is shown, while the initial 0.4 seconds is shown to the right. The 1D SPICE and 3D CFD-ACE models predict slightly faster temperature drop than the 2D ANSYS model. This is expected as the thermal mass in the ANSYS model is larger due to differences in the thickness of the lid in the models.*

The left of figure 2.16 shows simulation of the cooling at the thermometer for the first 2 seconds after power to the heaters has been turned of, while the right side shows the first 0.4 seconds. Due to the differences in lid thickness and thus in the total thermal mass, the 1D SPICE model and the 3D CFD-ACE models predict slightly higher cooling rates than the 2D ANSYS model, especially at the beginning of the cooling step. At later times the 2D ANSYS model and the 3D CFD-ACE model begins to approach each other with the 1D SPICE model predicting slightly faster cooling. The 1D SPICE

model and the 3D CFD-ACE model predicts an average cooling rate between 90°C and 80°C of ∼40°C/s. The 2D ANSYS model predicts a cooling rate when a thicker lid is used of ∼35°C/s. All 3 models predicts an average cooling rate of ∼20°C/s for the temperature transition from 90°C to 60°C. The predicted cooling rates for the models are summarized in table 2.4.

The effect of the bond layer for the lid has been omitted in all the models. This assumption is valid for the thin SU-8 to SU-8 bonding but may not be valid in cases were PDMS bonded lids are used. In configurations where the bond layer thickness is not negligible the influence of the bond layer is similar to a difference in lid configuration and a small effect on the initial cooling rate can be expected.

Table 2.4: *Simulated cooling rates for PCR chip*

Simulation model	1D SPICE	2D ANSYS	3D CFD-ACE
Average cooling rate 90°C → 80°C [°C/s]	∼40	∼35	∼40
Average cooling rate 90°C → 60°C [°C/s]	∼20	∼20	∼20

It takes 1.5 seconds to cool from the denaturation temperature of 94°C to an annealing temperature of 60°C at the position of the thermometer, according to the simulations. However, it has to be remembered that the cooling rates are dependent on the position in the PCR chamber. From the 2D ANSYS simulation in figure 2.7 on page 27 we have found that for a 1000μm thick substrate the average cooling rate between 90°C and 80°C at the substrate is approximately 3 times higher than at the top of the chamber. At the top of the chamber the cooling rate is only approximately 12°C/s. The average cooling rate at the top of the chamber for the transition from 90°C to 60°C is 10°C/s, which is about half the average cooling rate at the top of the substrate. It thus takes ∼3 seconds to cool from the denaturation temperature of 94°C to an annealing temperature of 60°C at the top of the PCR chamber.

2.5.5 Heating rates

The heating rates that can be achieved with the PCR chip design depend on the design of the power supply used. If heating is performed with twice the steady state power needed at 94°C, ∼11W, then a 2D ANSYS simulation predict a heating rate from 60°C to 90°C of ∼40°C/s at the position of the thermometer on the substrate. At the top of the chamber a heating rate of ∼15°C/s is predicted.

2.6 Summary

In this chapter the design of a SU-8 based PCR chip with integrated thin film platinum heaters and temperature sensor has been discussed. First the basic design was presented with a list of requirements the chip should fulfill. Then the design was validated

and optimized using PCR material compatibility tests and thermal simulations. Based on this a final PCR chip design was presented and the expected performance evaluated using thermal simulations. Two versions of the design were made when it was discovered that the heater configuration in the original implementation had negative implications for the temperature control of the chip.

Chapter 3

Fabrication and packaging of PCR chip

In this chapter the fabrication sequence for the PCR chip is presented. Two versions of the PCR chip have been fabricated, version 1 and version 2. The fabrication process for the two versions is identical except for the metallization mask, because the two versions only differ in the thin film heater layout. The silanization procedure for making the chips PCR compatible is also described as well as the methods of bonding lids to seal the PCR chamber. Finally the packaging of the chips is presented.

3.1 Fabrication

The mask layout for the fabrication of version 2 of the PCR chip is shown in figure 3.1. Mask 1 is the metallization mask for defining the thin film heaters and temperature sensor. Mask 2 defines the thin layer that protects the thin film heaters, while mask 3 defines the PCR chamber walls. Mask 1 is a clear field mask, while mask 2 and mask 3 are dark field. The masks for version 1 of the PCR chip are identical except for a a small difference in the metallization mask. The fabrication process is described in the next section, while the detailed process sequence can be found in appendix B.

4 inch Borofloat glass wafers from Schott [84] with a thickness of 1mm are used as substrate, see figure 3.2a. The wafers are cleaned using Triton X100 on a turn-table and rinsed in water. After this the wafers are cleaned again using Piranha (4:1 H_2SO_4:H_2O_2) and rinsed in water once more.

The platinum thin film heaters and temperature sensor are structured using a lift-off process. To improve resist adhesion to the Borofloat wafers a 20nm aluminum layer is e-beam evaporated onto the wafers. A 1.5μm thick AZ5214E resist is spun onto the wafer and patterned using the image reversal lithography process and the metallization mask, mask 1 in figure 3.1. Exposed aluminum from the adhesion layer not removed during the development of the resist, is removed by an aluminum etch (2:1 H_3PO_4:H_2O). The resist is hardbaked on a 120°C hotplate for 2 minutes, whereafter

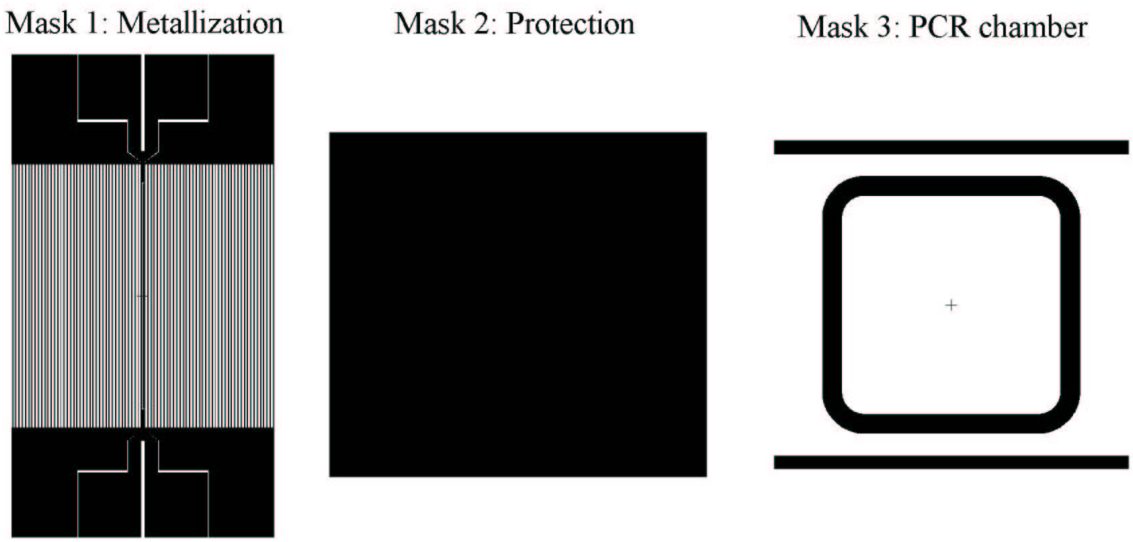

Figure 3.1: *Mask layout for PCR chip version 2. Mask 1 is for metallization, mask 2 is for protection of the electrodes and mask 3 is for definition of the PCR chamber. Mask 1 is a clear field mask, mask 2 and mask 3 are dark field masks.*

200nm of platinum is deposited using e-beam evaporation with a 100Å titanium adhesion layer. If the resist adhesion is poor the resist will start to peel of during the deposition of platinum. The platinum is structured using lift-off in a ultra-sonic assisted acetone bath for 5 minutes. After this the rest of the aluminum adhesion layer is stripped in the aluminum etch and the platinum heaters and thermometer of the PCR chip have been defined, see figure 3.2b. In figure 3.3 is shown an optical image of the heater and thermometer electrodes of both version 1 and version 2 of the design. In version 1 to the left in the figure there is double heater spacing at the position of the thermometer, whereas the in version 2 to the right in the figure the heater spacing is continuous and the thermometer is embedded between the heaters.

A thin layer of SU-8 is used to protect the thin film electrodes. To improve the adhesion of SU-8 the wafers are dehydrated by baking in a 250°C oven for more than 3 hours prior to the spinning of SU-8. Immediately after the wafer has cooled a 5μm SU-8 layer (XP2005, Microchem [85]) is spun onto the wafer with a rotation speed of 3000 rpm. The resit is soft baked for 3.5 minutes at 90°C and patterned by exposure through the PCR protection mask, mask 2, followed by a cross link bake. The cross link bake is done on a hotplate ramped from room temperature to 95°C in 5 minutes, staying at 95°C for 8 minutes, ramping to 105°C in 2 minutes and staying at this temperature for another 10 minutes. The wafers are left to cool on the hotplate for the approximately 60 minutes it takes to reach room temperature. Figure 3.2c shows the cross linked part of the SU-8 protective layer. In figure 3.4 an optical image of a PCR chip with bad adhesion of the protective layer is shown. Bad adhesion of the protective layer was the most common failure mechanisms during the fabrication of the

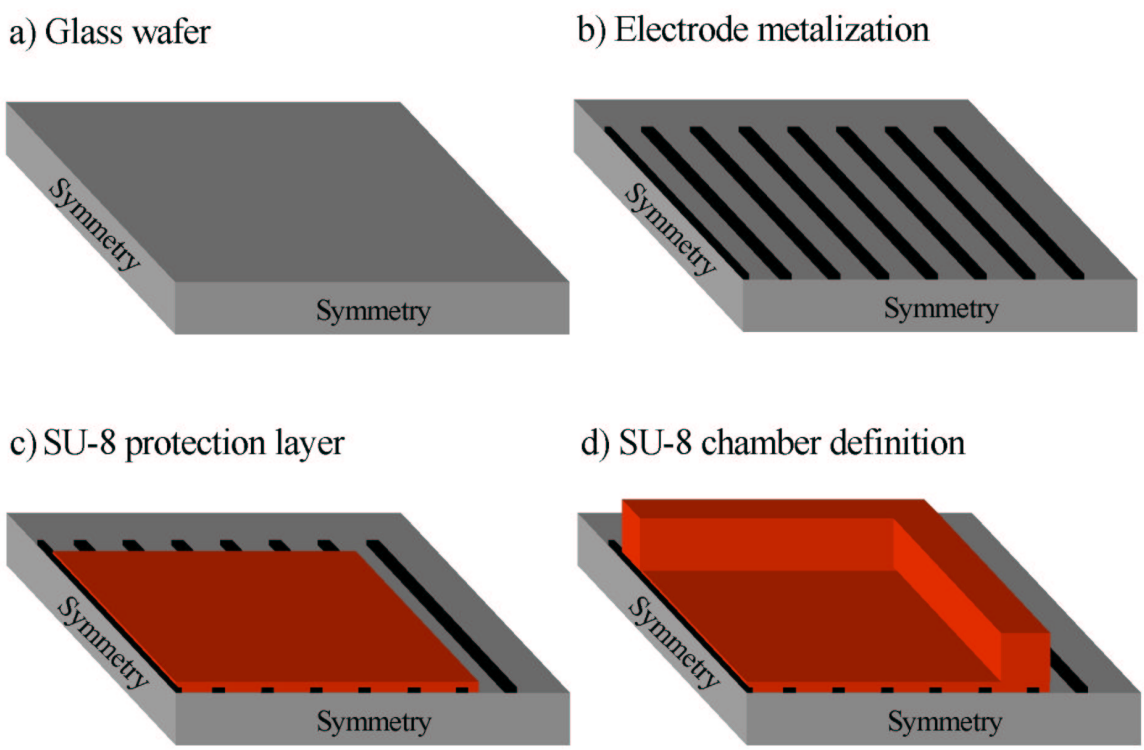

Figure 3.2: *Schematic of the process sequence for the PCR chip. Only one quarter of the chip is shown due to 2-fold symmetry in the design. The chip is realized using a simple 3 mask-layer process.*

PCR chip. The failures could be due to insufficient dehydration baking of the wafers prior to the SU-8 spin as well as due to insufficient cleaning of the wafers.

The final step in the process is to define the SU-8 chamber walls. This is done with a multi spin procedure to achieve a 400μm thick SU-8 layer. 200μm SU-8 (XP2075, Microchem [85]) is spun onto the wafer using a rotation speed of 1000 rpm and then soft baked on a hotplate for 45 minutes at 95°C using a temperature ramp of 10 minutes. The wafer is cooled on the hotplate until room temperature is reached. The spin and bake procedure is the repeated once more to realize a layer with a total thickness of 400μm. The chamber walls are defined by exposure through the PCR chamber mask, mask 3, followed by a cross link bake for 35 minutes at 95°C using a temperature ramp of 10 minutes to reach the bake temperature. Again the the wafer is cooled on the hotplate until room temperature is reached. Finally, the SU-8 is developed in PGMEA for approximately 30 minutes and the chip has been realized, see figure 3.2d. In figure 3.5 an optical image of a final PCR chip is shown.

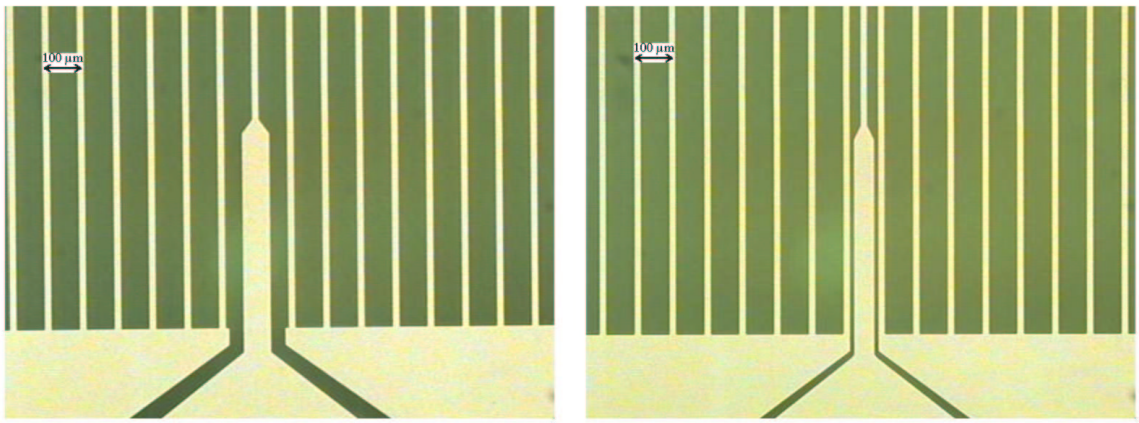

Figure 3.3: *Optical image of the thin film platinum heaters and thermometer for both version 1 and version 2 of the PCR chip design. To the left version 1 is shown and the double heater spacing at the position of the thermometer can be observed. In version 2, to the right, the heater spacing continuous to be 100 µm, even at the position of the thermometer.*

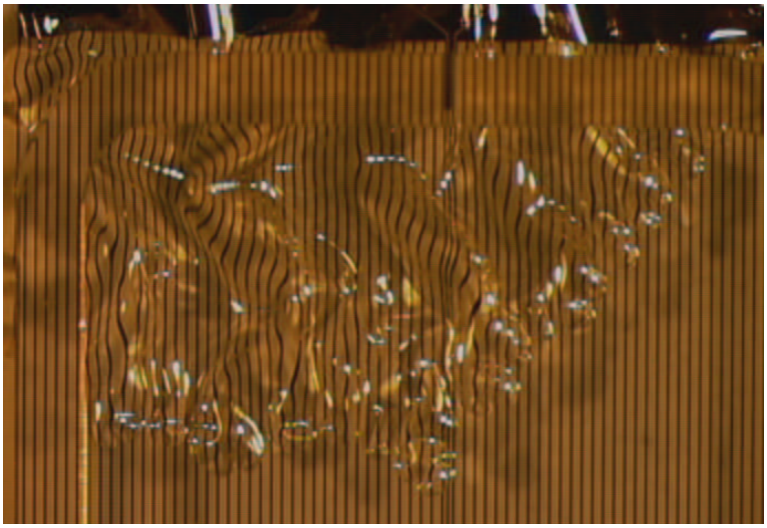

Figure 3.4: *Optical image of a PCR chip with poor adhesion of the SU-8 protective layer. At places with poor adhesion the SU-8 layer buckles and the chip is no longer functional.*

3.2 Silanization of PCR chip

The PCR compatibility tests of materials shown in table 2.1 on page 18 showed that untreated SU-8 inhibits PCR. It is therefore necessary to passivate the SU-8 surfaces in the chamber with a silanizing agent. A gas phase silanization using dichlorodimethylsilane has been used. A schematic of the setup is shown in figure 3.6. The PCR chips are

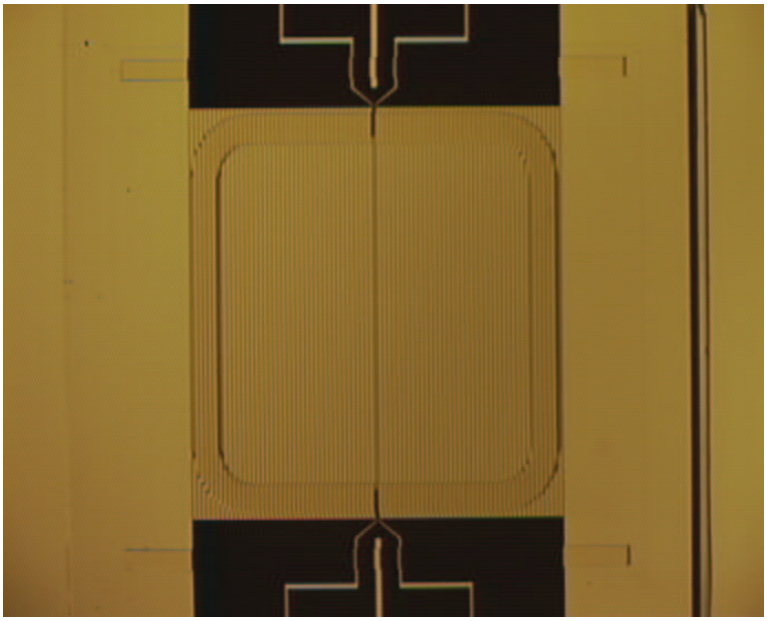

Figure 3.5: *Optical image of a PCR chip.*

placed in a silanization primer containing a beaker with dichlorodimethylsilane. After 1 hour exposure to the silane vapor the chips are taken out and washed in deionized (DI) water.

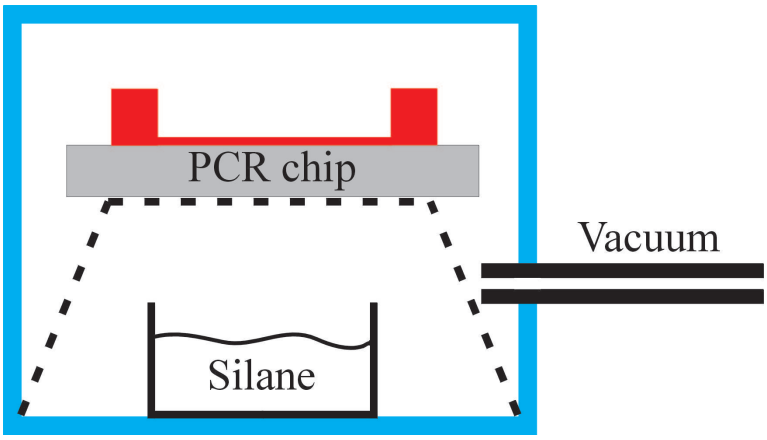

Figure 3.6: *Schematic of the gas phase silanization setup. The chip is placed in a silanization primer with a liquid dichlorodimethylsilane source. After exposure to the silane vapors for one hour the surface treatment is finished.*

3.3 Bonding of lids

Two methods have been used for sealing of the PCR chamber: SU-8 to SU-8 bonding and PDMS bonded lid. The lids are bonded on a chip to chip basis. With PDMS bonded lid the bond is reversible which makes fluidic handling simple as the chamber can be filled or emptied by removing the lid. However, a constant pressure has to be applied to keep the PDMS bonded lid tight. The application of this pressure has been made an integral part of the packaging of the PCR chip and will be described in the next section. In this section the fabrication of SU-8 bonded lids will be described.

The fluid interconnects have to be made either through the substrate or the lid when using SU-8 bonded lids. We have chosen to drill holes in the glass lid. After the holes have been drilled the glass lids are dehydrated on a hotplate at 200°C for 10 minutes and then a thin layer of SU-8 XP2005 is spun onto the lid at 4000 rpm. The SU-8 layer is partially soft-baked for 5 minutes at 80°C. The lid is then manually placed on top of the PCR chip applying a gentle pressure to facilitate the bond. The SU-8 PCR chamber on the PCR chip has been treated with an oxygen plasma making the surface hydrophillic to increase the wetting during the bond. After positioning of the lid the soft-bake is continued on the hotplate at 80°C for 30 minutes to complete the soft-bake of the SU-8 bond layer. After this the chip is UV exposed and the bond completed by a cross link bake of the chip at 90°C for 30 minutes.

In figure 3.7 optical images of chips with SU-8 bonded lids are shown. In the image to the left a closeup of the interface between the SU-8 chamber wall and the SU-8 bond layer is shown. It is seen that in some localized positions solvent from the bond layer can be trapped. However, even with some solvent trapped at the interface the bond will still make a tight seal in most cases. In the image to the right one of the two through holes for fluidic connection drilled in the lid is visible.

The yield of the SU-8 bonded lids is less than 50% and the fabrication process is very tedious and time consuming. Furthermore use of SU-8 bonded lids is not compatible with the gas phase silanization, described in the previous section, to make the surfaces of the chamber PCR compatible. A liquid phase silanization can be used in connection with SU-8 bonded chips, but has not been implemented. Therefore only a few test chips have been made with SU-8 bonded lids. Most of the chips fabricated have used PDMS bonding of the lids, which will be described in the next section.

3.4 Packaging

Almost all chips produced have used a PDMS bonded lid, because of easier fabrication and fluidic handling than with SU-8 bonded lids and because it is more suited for the gas phase silanization. PDMS bonded lids consist of a polymer or glass lid with a thin layer of PDMS. The lids are pressed against the PCR chamber to achieve a tight

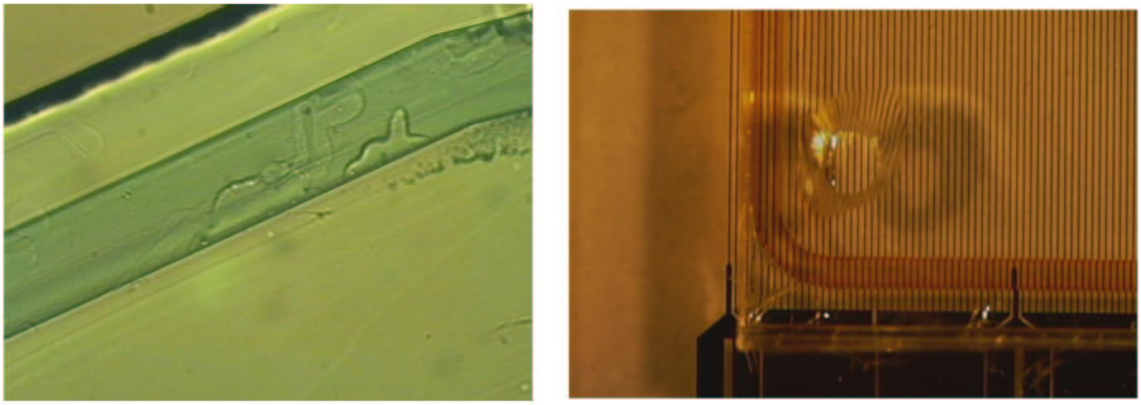

Figure 3.7: *Optical images of SU-8 bonded glass lids. To the left a close up of the bond interface. Some solvent from the SU-8 bond layer has been trapped, but the seal is still intact. To the right one of the through holes for fluid connection drilled in the lid can be seen.*

seal. The application of this pressure has been made an integral part of the packaging of the PCR chip. Packaging of the PDMS bonded PCR chips also involves making electrical connections to the chip as well as connecting the PCR chip to a heat-sink with good thermal contact. Two methods of packaging have been used which mainly differ in the way the electrical connection to the chip is performed. One method, the pogo pin setup, offers a simple scheme for the electrical interconnection. However with this packaging method the optical access to the PCR chamber is restricted. In the other method, chip carrier setup, there is optical access to the PCR chamber, but the electrical interconnection is more cumbersome and requires an expensive ceramic chip carrier. Optical access to the PCR chamber is only needed for experiments where fluorescent probes are used for characterization of the performance.

3.4.1 Pogo pin packaging setup

A schematic of the pogo pin packaging setup is shown in figure 3.8. The PCR chip is placed in a recess made in an aluminum block. The aluminum block acts as the heat-sink for the PCR chip, and to achieve good thermal contact heat conducting paste can be applied between the chip and the heat-sink. Pressure for the PDMS bonded lid is provided via a PMMA pressure support plate using spring mounted screws. The PMMA pressure support is structured so that it only pushes near the edge of the lid, to minimize the influence on the thermal properties of the chip and also to provide better optical access to the PCR chamber. Electrical connection to the chip is made through pogo pins (SS-30-J-1-1.3-g, Interconnect Devices [86]) placed in the PMMA support structure and aligned to bond pads on the chip. Wiring to the power supply and temperature control systems can then easily be made through jacks to the top of the pogo pins.

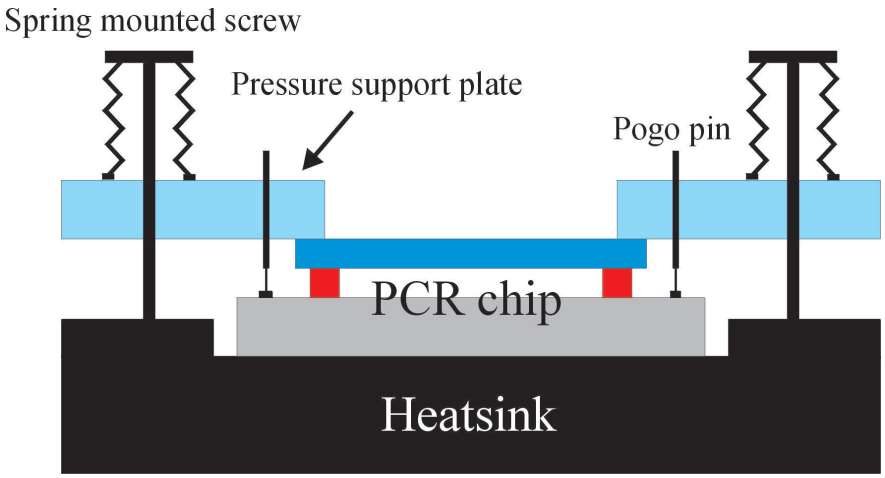

Figure 3.8: *Schematic of the pogo pin packaging setup. The PCR chip is placed in a recess on an aluminum block which acts as a heatsink. Pressure to the PDMS bonded lid is provided via a PMMA pressure support plate using spring mounted screws. Electrical connection is made throug pogo pins positioned in the PMMA support plate and aligned to bond pads on the chip.*

The electrical connection scheme in the pogo pin setup is very easy as the connections are made automatically with bonding of the lid. But because the pogo pins used for the electrical connections are accessed from the top, the pins and the wires tend to restrict the optical access to the PCR chamber. The access is not blocked by the packaging, but the is not enough space to place a microscope objective directly above the PCR chip.

3.4.2 Chip carrier packaging setup

A schematic of the chip carrier packaging setup is shown in figure 3.9. The chip is positioned in a ceramic chip carrier (MCPG14434, Spectrum Semiconductor materials [87]) that will provide the electrical connection to the chip as well as thermal contact to a heat-sink. The electrical connection between the chip carrier and the PCR chip is made by wire-bonding from bond pads on the chip carrier to bond pads on the chip. The chip carrier is then positioned on an aluminium block that acts as heat-sink. To achieve good thermal contact heat conducting paste can be applied between chip and chip carrier and between chip carrier and heat-sink. The aluminum block is structured so that the pins on the chip carrier can be accessed. As with the pogo pin setup pressure for the PDMS bonded lid is provided via a PMMA pressure support plate using spring mounted screws. The PMMA pressure support is again structured so that it only pushes near the edge of the lid to minimize the influence on the thermal properties of the chip and also to provide better optical access to the PCR chamber.

Because the electrical interconnects and wiring are on the bottom in the chip carrier packaging setup, the top side is free of restrictions and a microscope objective can now

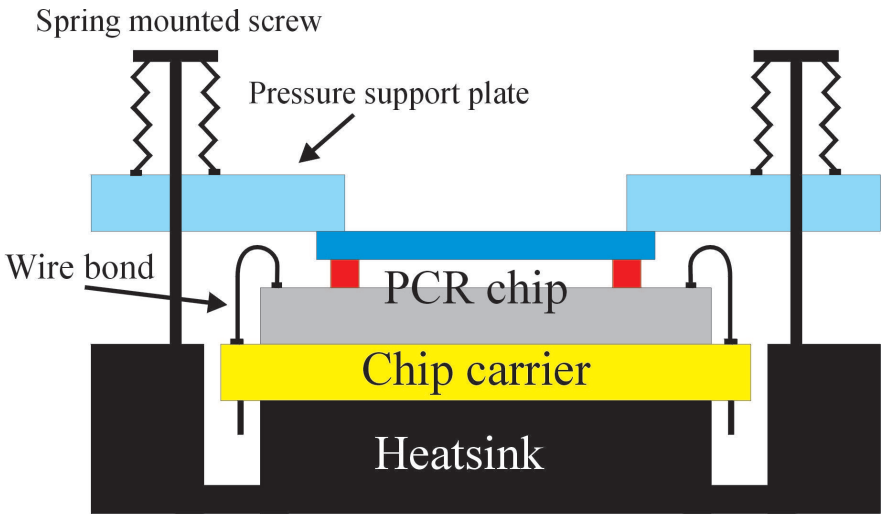

Figure 3.9: *Schematic of the chip carrier packaging setup. The PCR chip is placed in a ceramic chip carrier which provides electrical connection to the chip as well as contact to a heat-sink. The electrical connection between the chip carrier and the PCR chip is made by wire-bonding. The chip carrier is placed in a structured aluminium block that acts as a heat-sink. Pressure to the PDMS bonded lid is provided via a PMMA pressure support plate using spring mounted screws.*

be positioned directly above the lid for optical access to the PCR chamber. However, the wire-bonding step makes the electrical interconnection more cumbersome than in the pogo pin packaging setup and the use of a relatively big and expensive ceramic chip carrier adds to the cost of the packaging.

3.5 Summary

The fabrication process for the PCR chip has been described in this chapter for version 1 and version 2 of the PCR chip design. The actual fabrication of the chip is identical for the two versions and was done using a relatively simple 3 layer process. After fabrication, silanization of the chip was performed to enhance the PCR compatibility of the chip. A procedure to seal the chamber using a PDMS bonded lid and to package the chip with electrical connection and connection to a heat-sink has been presented. A more complicated process for realizing SU-8 bonded lids was also presented. Almost all of the fabricated chips have used PDMS bonded lids.

Chapter 4

Characterization of PCR chip

In this chapter the characterization of the PCR chip will be described. The characterization will include both physical performance of the PCR chip, such as power consumption and cooling rates, as well as analysis of the PCR amplicon to test the efficiency of the chip for PCR amplification. The physical performance will be compared to the predictions from thermal simulations of the design in chapter 2 and to literature studies of other PCR chips. PCR efficiency will be compared to the performance of conventional PCR performed in tubes using a commercially available thermocycler. Other results and detailed information about the bio assays can be found in [83]. All results presented are from version 2 of the design, except in section 4.2.5 where results from version 1 of the design have been included to illustrate the effect differences in heater configuration in the two designs has on the temperature control of the PCR chip.

4.1 Setup

For thermal measurements and for PCR amplification the chip setup uses the pogo pin packaging method shown in figure 3.8 on page 46. This packaging scheme offers easy electrical connection to the chip, but is not suitable when optical access to the PCR chamber is needed. Thermocycling is performed using a ∼15W custom-built power supply with a LabView based PID controller and data acquisition system. Detailed information about the setup can be found in [88]. A picture of the pogo pin setup and the power supply system is shown in figure 4.1.

For measurements with fluorescent probes the chip carrier packaging method shown in figure 3.9 is used. With this packaging scheme wire bonding is used for electrical connection. The chip carrier setup is the positioned in a microscope setup for fluorescent measurements.

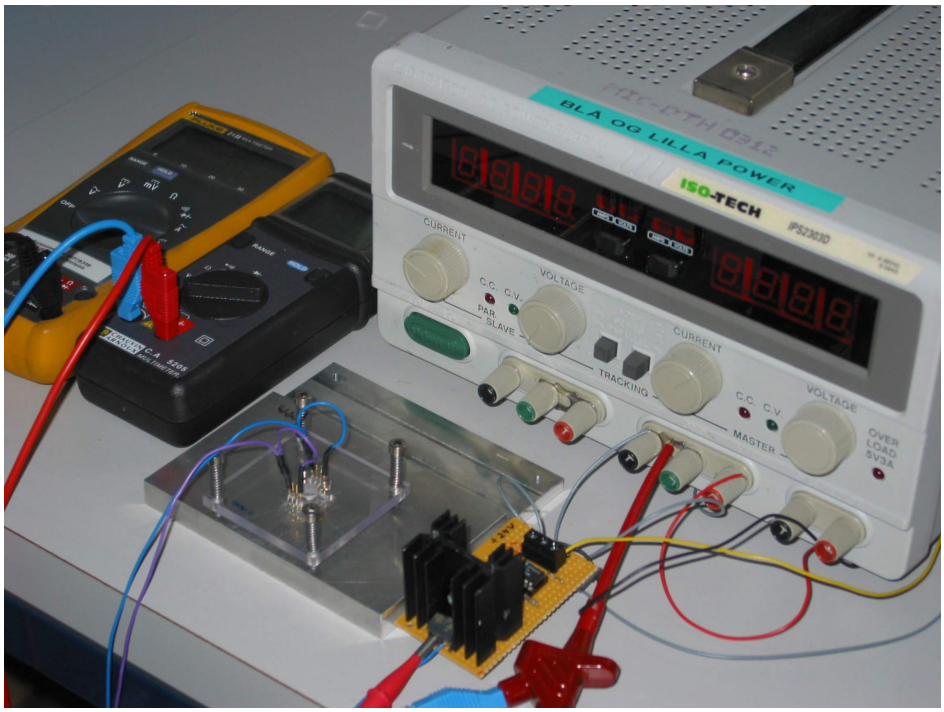

Figure 4.1: *Optical image of the setup used for PCR thermocycling. The chip is packaged using the pogo pin setup. The thermocycling is performed using the ∼15W power supply system and a Labview based control system.*

4.2 Physical characterization

In this section the physical performance of the chips will be characterized. This will include both power consumption and cooling rates, but also an evaluation of the temperature control using the build in resistive thermometer. The results will be compared to the simulations of the PCR chip found in the design and simulation chapter. The chips tested all used a 500μm glass lid with a PDMS bond layer.

4.2.1 Calibration of integrated thermometer

Before use, the build in resistive thermometer is calibrated. This is done in a temperature controlled oven, where the resistance of the thermometer is measured at different temperatures between room temperature and 100°C. The calibration curves are then stored in the computer and used by the Labview based controller program to convert resistance measurements into temperature readings during operation of the PCR chips. Figure 4.2 shows the obtained calibration curves for 3 different chips.

From figure 4.2 is is seen that the resistance of the build in thermometer varies linearly with temperature. The behavior can be described by equation 4.2-1.

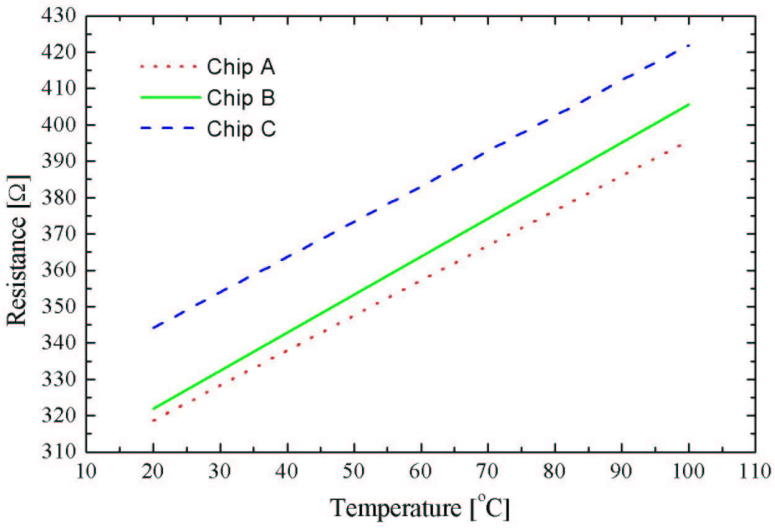

Figure 4.2: *Calibration curves for the build in resistive thermometer from 3 different PCR chips*

$$R(T) = R_0 \left[1 + (T - T_0)\alpha\right] \tag{4.2-1}$$

α is the temperature coefficient of resistance (TCR). The three examples of calibration curves in figure 4.2 have almost identical slopes, corresponding to a TCR value of $\alpha \sim 29 - 32 * 10^{-4} C^{-1}$. This is slightly lower than the $\alpha \sim 39 * 10^{-4} C^{-1}$ value found in literature [89], presumably due to differences in the purity of the materials. The different offset of the thermometers is caused by thickness variations in the platinum across a wafer and from batch to batch.

4.2.2 Power consumption

The power consumption of the chip is dependent on the thermal contact between the chip and the heat-sink. To assure good thermal contact heat conducting paste was used between the chip and the heat-sink. The total power needed to heat the PCR chip to a temperature of 94° was measured to be ∼6.3W. This is slightly higher than the power consumption predicted by the thermal simulations in chapter 2, but this figure includes power loss in the on-chip interconnects leading to the heater arrays. The power loss in the on-chip interconnects depends on the resistance of the interconnects relative to the resistance in the heater arrays and can be estimated by geometrical considerations to be approximately 10 % of the total power dissipated on the chip. When this loss is subtracted the power consumption actually used to heat the PCR chamber is estimated to 5.7W which also is the power consumption predicted by the 3D FEM ANSYS and CFD-ACE simulations of the design. The power consumption of the PCR chip is

approximately a factor 3 higher than typical silicon micromachined PCR chips with a similar size chamber reported by other research groups [26]. However, the power consumption of the chip is very dependent on the chamber size and if needed lower power consumption can be obtained by using smaller PCR chambers.

4.2.3 Cooling rates

In figure 4.3 is shown a measurement of the temperature drop of the PCR chip from 90°C when the power to the heaters are turned off. The temperature is measured by the build in resistive thermometer. 2D ANSYS and 3D CFD-ACE simulations of the temperature drop are also included in the figure. The predicted cooling rates from simulations can be found in table 2.4 on page 37. The thermal properties of the lid configuration of the tested chips using the PDMS bonded 500μm glass lid and the pogo pin packaging is different than for the simulated chips where the influence of the bond layer and the packaging have been omitted. According to the simulations in chapter 2 the effect of small differences in lid configuration on the cooling rates should be minimal and limited to the initial maximum cooling rate. The lid thickness in the CDF-ACE simulation was 500μm whereas the ANSYS model used a 750μm glass lid.

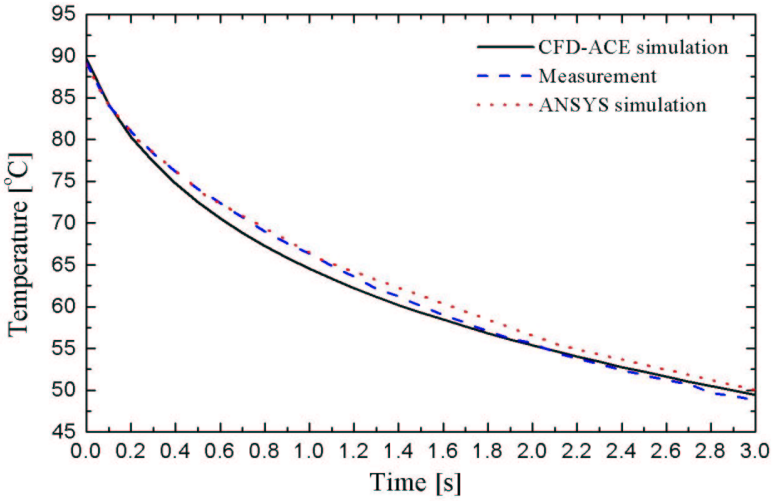

Figure 4.3: *Measurement of the temperature drop from 90°C. Included in the figure are CFD-ACE and ANSYS FEM simulations of the temperature drop. There is good agreement between the FEM models and the measurement, despite small differences between the lid configuration in the measurement setup and the FEM models.*

The initial measured temperature drop of the PCR chip in figure 4.3 is slightly slower than the CFD-ACE simulations and corresponds better to the ANSYS simulation. At later times there is good agreement between the measured temperature drop and both

FEM simulations and an average cooling rate between 90°C and 60°C of ∼ 20°C/s is found. The effect of the of the PDMS bond layer, and the pogo pin packaging which have been omitted in the modelling of the PCR chip is thus as expected limited to a small drop in the initial cooling rate. The overall performance of the PCR chip is still close to the performance predicted by the simulations. The measured and simulated cooling rates are summarized in table 4.1.

The temperature drop from 90°C to 60°C corresponds to the typical temperature transition between denaturation temperature and annealing temperature in a PCR cycle and is an important measure of the performance of the PCR chip. The ∼ 20°C/s average cooling rate of the PCR chip is a order of magnitude higher than for conventional PCR cyclers that normally only reach a cooling rate of a few degrees per second. The cooling rates reported in literature for other PCR microchips lies in the range from 5°C/s all the way up to 70°C/s depending on the design and cooling method. Silicon based devices and devices with active cooling are generally fastest [22, 23] while polymer devices lie in the lower range [34] for cooling rates. Some of the glass based chips have cooling rates similar to our PCR chip [45]. It is not always clear if the quoted values are average cooling rates or maximum cooling rates or if they are measured on the substrates or in the chamber, making comparison of cooling rates difficult. The performance of our chip seems to be comparable with some of the best silicon micromachined PCR chips.

Table 4.1: *Measured and simulated cooling rates for PCR chip*

		ANSYS	CFD-ACE	Measured
Average cooling rate 90°C → 80°C	[°C/s]	∼35	∼40	∼30
Average cooling rate 90°C → 60°C	[°C/s]	∼20	∼20	∼20

4.2.4 PCR thermocycling

In the setup PCR temperature cycling was controlled by a Labview based PID controller. If the settings of the PID controller are conservative the rate of the transition between set points will be slow but stable. If the settings are aggressive the transition between setpoints will be faster, but at the risk of overshooting the setpoint. In figure 4.4 a PCR cycle with fast temperature response almost without overshoot is shown.

The transition time from 92°C (denaturation) to 57°C (annealing) is just under 3 seconds, with approximately half of this time used to correct the initial miss of the setpoint, figure 4.4. The transition time from the anneal temperature 57°C to the extension temperature 70°C is approximately 1 second, as is the transition time from 70°C to 92°C between extension and denaturation temperature. The maximum heating rate achieved during the transitions is approximately 50°C/s when using up to 15W power input. The PCR chip is thus capable of very fast thermal cycling, with transition

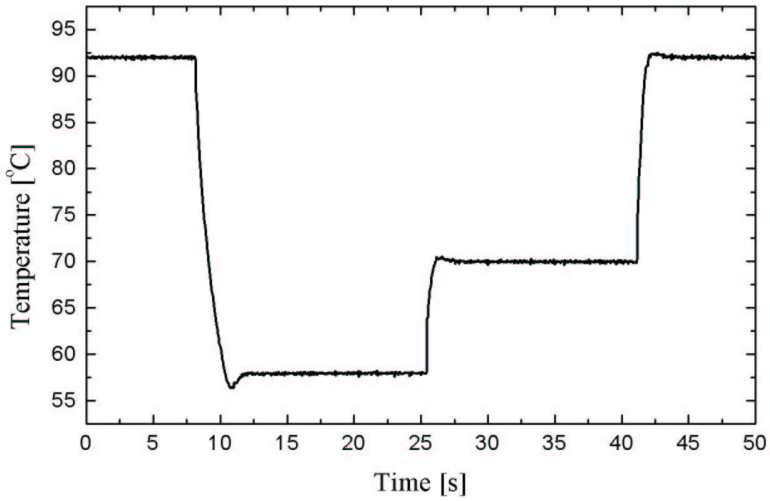

Figure 4.4: *Example of a PCR thermocycle with PID control settings that gives fast temperature response and small overshoot of temperature setpoints. The PCR chip is capable of fast thermal cycling, with total transition time between setpoints accounting for as little as 5 seconds per PCR thermocycle.*

times accounting for as little as 5 seconds per PCR thermocyle. However if extremely short dwell times at each setpoint are used it has to be remembered that the transitions are measured at the position of the thermometer and that the transitions at the top of the PCR chamber according to the simulations are slower.

4.2.5 Temperature control

To test how accurate the temperature control within the chip is when the integrated temperature sensor is used, we performed a melting curve experiment with Campylobacter gene cadF PCR product using SYBR green I as fluorescent dye. Melting curve experiments can be used to find the melting temperature T_m of the target DNA, which is the temperature where 50 % of the DNA is double stranded while the other 50 % of the DNA has denaturated into single strands. Because SYBR green only fluoresces when it is bound to double stranded DNA, the melting temperature can be found by measuring the fluorescent emission at different temperatures. DNA melting is observed as a sudden decrease in the fluorescence [69]. The melting temperature T_m can also be estimated in a conventional PCR thermocycler by performing PCR denaturation temperature gradient experiments. In these experiments a series of PCR amplification cycles with different settings of the denaturation temperature is performed. Amplification of PCR product will only occur when the denaturation temperature is high enough for melting of the DNA.

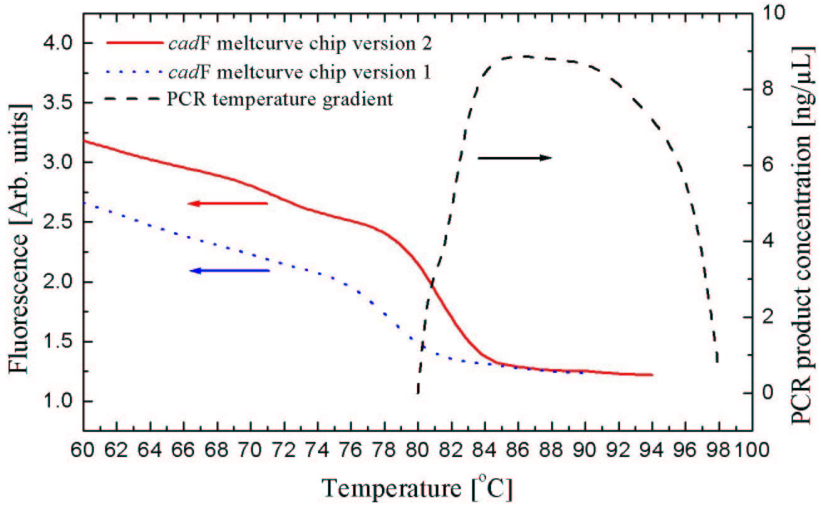

Figure 4.5: *Melting curve and PCR temperature gradient experiments of* cad*F. A melting temperature T_m of ∼82°C and ∼82.5°C is found from the melting curve experiment using the final PCR chip design and from the PCR temperature gradient experiments respectively. A melting temperature T_m of ∼78°C is found from the melting curve using the old design. The 4°C offset is due to the poor heater configuration in the old design and corresponds to the offset predicted by simulations.*

In figure 4.5 the melting curves from cadF PCR product using both version 1 and version 2 of the PCR chip design is shown. Included is also the results of PCR denaturation temperature gradient experiment using a conventional PCR thermocycler. The melting curve experiment from the final PCR chip shows an onset of melting at just under 80°C and that melting is completed at 85°C. This corresponds to a melting temperature T_m of cadF of ∼ 82°C. The PCR denaturation temperature gradient experiments shows amplification of PCR products beginning at a denaturation temperature just over 80°C with maximum PCR product reached at a denaturation temperature of 85°C. At higher denaturation temperatures the PCR product formation starts to decrease because of increased inactivation of the enzyme. The result of the PCR denaturation experiments corresponds to an estimated melting temperature of cadF of 82.5°C. The good agreement between the melting curve experiments using the final PCR chip design, version 2, and the PCR thermal gradient experiments shows that the temperature control of the chip is accurate as predicted by the thermal simulations in chapter 2. The 4°C temperature offset at the position of the thermometer in design version 1 predicted by the simulations in section 2.5.3 is also seen in the melting curve experiment. The melting temperature of cadF found using the old design is approximately 78°C according to the temperature reading from the chip, which is ∼ 4°C lower than the value found using the final PCR chip design.

4.3 PCR amplification

Initial testing of PCR amplification in the chips was performed by amplification of a 199 base pair fragment of yeast ribosomal S3 gene using a hotstart Taq polymerase. These tests used PCR chips with untreated SU-8 surfaces, which according to the PCR compatibility tests in chapter 2 has poor PCR compatibility. It was also found that PCR amplification in these chips was only possible by using 10 times the normal Taq polymerase content and that the results were not reproducible. Due to the high cost of Taq polymerase, it would be preferable to avoid the need of an increased amount of Taq polymerase. To achieve this a silanizing agent, dichlorodimethylsilane, was used to chemically treat the SU-8 surfaces, which according to our PCR compatibility tests results in a PCR compatible surface.

The PCR compatibility of the silanized PCR chambers was tested by amplification of *Campylobacter* gene *cad*F using standard AmpliTaq DNA polymerase. A polymerase content of 1 unit in the 20 μL PCR chamber was used, which is only twice the concentration of Taq polymerase recommended by the supplier for conventional PCR. All samples were analyzed using an Agilent bioanalyzer 2100 with a DNA 500 chip kit.

4.3.1 PCR amplification in dummy chip

To test the performance that could be achieved with the silanized PCR chips compared to conventional PCR systems, PCR was performed under identical conditions using a standard flatbed thermocycler to perform the thermocycling of the chip. For this purpose dummy PCR chips, where only the PCR chamber part of the chip has been fabricated, were used. The PCR amplification was performed using 40 cycles, with 1 minute denaturation at 94°C, 1 minute annealing at 45°C and 3 minutes extension at 72°C. A 5 minute hotstart at 94°C was used in the first PCR cycle.

In figure 4.6 two superimposed electropherograms of the analysis of a PCR amplification of cadF done in both silanized PCR chips and in conventional PCR tubes under the same conditions are shown. The peak at 78s in the electropherogram is the PCR product while the smaller peak at 90s is an internal marker from the bioanalyzer used for calculation of DNA size and concentration. The concentration of the PCR amplicon in conventional PCR tubes was 18 ng/μl whereas PCR in chips gave a concentration of 12 ng/μl. The yield of PCR product in chips is thus $\sim$2/3 of the yield in conventional tubes when performed under identical conditions. Not many quantitative comparisons between PCR amplification in chips and conventional PCR tubes exist in literature. A similar value of 60 % was found by Liu *et al.* [34]. In many cases it is not interesting to perform the analysis in the PCR chip using the same conditions as in conventional PCR thermocyclers, as the reason for using PCR chips is not based on the amount of amplicon produced but the ability to perform the amplifications faster or with smaller volumes.

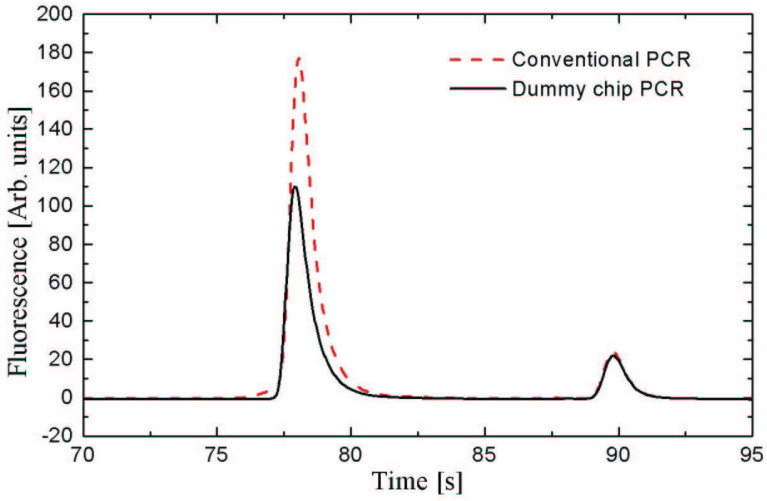

Figure 4.6: *Two superimposed electropherograms from an Agilent bioanalyser showing the analysis of PCR amplification of* cad*F done in PCR chip and conventional PCR tubes. The PCR has been performed under identical conditions and the yield of PCR product in chip is ∼ 2/3 of the yield in conventional PCR tubes.*

4.3.2 PCR amplification in PCR chip

When doing PCR amplification using the real PCR chips the heating and cooling rates are very different from that of conventional PCR systems. PCR thermocycling can be performed faster in the PCR chips which results in lower overall amplification time. Using the same extension time of 1 minute, but with 15 seconds anneal and denaturation time in PCR chips compared to 30 seconds in the conventional thermocycler, PCR amplification was performed in both systems. The initial 5 cycles were performed with an denaturation temperature of 94°C, while the next 35 cycles were performed with a denaturation temperature of 85°C. The annealing temperature was 45°C and the extension temperature 72°C during all 40 cycles. The dwell times in the chip thermocycle do not represent the lower limit for the PCR chip, but are used because the obtained results were still reproducible.

The analysis of the PCR amplicon from the chip and the conventional PCR tubes are shown in figure 4.7. The yield of the PCR product in the PCR chip were approximately 50 % of the yield from the conventional PCR tubes. This is slightly lower than in the last section where the PCR was performed under identical conditions, but still very respectable. The lower yield can be due to the differences in anneal and denaturation times, an effect of the different heating and cooling rates, but could also be a result of the temperature drop that exists near the edge of the PCR chamber predicted by the thermal simulations in chapter 2. The performance of the PCR chip with the current

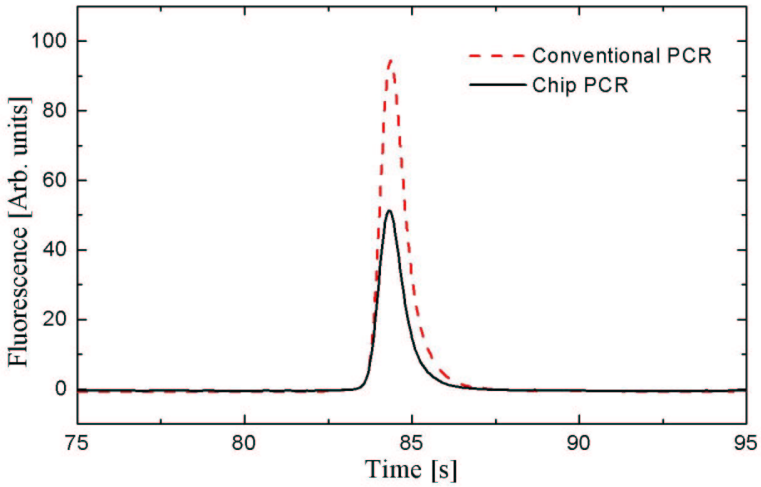

Figure 4.7: *Two superimposed electropherogram from an Agilent bioanalyser showing the analysis of PCR amplification of* cad*F done in PCR chip and conventional PCR tubes. The PCR amplification done in the chip used half the dwell time at denaturation and annealing temperatures as the PCR done in tubes. The yield of PCR product in the PCR chip is ∼50% of the yield from the conventional PCR tubes.*

bio assay is however still more than adequate and faster thermocycling still result in detectable PCR amplicon, at total amplifications times not obtainable with conventional thermocyclers.

The silanization coating procedure for the PCR chips is not completely stable and reproducible. There have been periods where the coating did not work properly, presumably due to degradation of the dichlorodimethylsilane source used for the silanization. However, in most cases by carefully following the silanization protocol an almost 100% yield can be achieved. Details about the coating aspects of the PCR chip can be found in [83].

4.4 Summary

In this chapter the performance of the PCR chip has been characterized. The thermal properties of the chip were measured and compared to simulations. There was excellent agreement between measurement and simulation of the thermocycling capabilities of the PCR chip, with heating and cooling rates in excess of 30°C/s, comparable with the best silicon micromachined PCR chips. It was found that silanization of the SU-8 surfaces in the PCR chamber enhances the PCR compatibility resulting in PCR chips performance comparable to that of conventional PCR tubes when performed under

identical conditions. The PCR chip continued to perform adequately even when a faster thermocycling than possible with conventional thermocyclers is used.

Chapter 5

Fabrication and test of DEP devices for cell handling

In this chapter fabrication and test of DEP devices for cell manipulation and cell characterization will be presented. The devices in this chapter will only include DEP functionality. The intended use as sample pretreatment system monolithically integrated with the PCR chip presented in the previous chapters, form the basis for some of the material and design choices of the devices. First DEP devices fabricated on silicon substrates are presented. These devices are used to test different sample pretreatment techniques prior to PCR, but also used to test general cell manipulation and characterization techniques. After validation of the functionality of the devices, fabrication of the DEP structures on glass substrates is presented, as this is needed for on chip integration with the PCR chip presented in the previous chapters.

5.1 Dielectrophoresis

Dielectrophoresis (DEP) is the motion of particles suspended in an aqueous solution caused by induced polarization effects in inhomogeneous AC electrical field. For a spherical particle with absolute permittivity ε_p^* and radius r suspended in a medium with absolute permittivity ε_m^* the DEP force F_{DEP} is given by equation 5.1-1 [48, 90, 91]

$$F_{DEP} = 2\pi r^3 \varepsilon_m \alpha_r \nabla E^2 \quad , \quad \text{where} \quad \alpha_r = \text{Re}\left[\frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*}\right] \quad \text{with} \quad \varepsilon_i^* = \varepsilon_i + \frac{\sigma_i}{j\omega} \quad (5.1\text{-}1)$$

ε_i is the permittivity and σ_i is the conductivity of the particle or the surrounding media. α_r is the real part of the Clausius-Mossotti factor and defines the effective polarisability of the particle relative to the surrounding media. It depends on both the cell type, the angular frequency ω of the applied field and the conductivity and permittivity of the surrounding media. If $\alpha_r > 0$, the DEP force will be directed towards the region of high field gradient and this is called positive dielectrophoresis or p-DEP. If

$\alpha_r < 0$, the DEP force will be directed towards the region of lowest field gradient and this is called negative dielectrophoresis or n-DEP. The region of highest field gradient always occurs at the electrode edges while the field minima can exist away from the electrodes or on top of the electrodes.

Conventional DEP utilizes stationary AC fields. However, two related techniques uses a moving electrical field either in form of a electrorotation (ROT) or travelling electrical field (TWD). Because the build up and decay of the induced dipoles takes a certain amount of time interactions between the induced dipole and the moving field can result in a torque acting on the cell, given by [90, 91, 92]

$$\Gamma = -4\pi r^3 \varepsilon_m \alpha_i E^2 \quad , \quad \text{where} \quad \alpha_i = \text{Im}\left[\frac{\varepsilon_p - \varepsilon_m}{\varepsilon_p + 2\varepsilon_m}\right] \quad \text{with} \quad \varepsilon_i^* = \varepsilon_i + \frac{\sigma_i}{j\omega} \qquad (5.1\text{-}2)$$

If the particle is under the influence of n-DEP, then the induced torque can result in rotation of the particle in the case of ROT or translational motion of the particle in the case of TWD [92]. If the particle is under the influence of p-DEP, then the particle will be immobilized at the electrode edges.

Because the polarisability of a particle can change with the frequency of the applied field and because the response depends on the specific particle, DEP is a very useful technique for characterization and manipulation of cells. Typical electrode geometries and methods for cell manipulation and sample treatment were presented in section 1.2 on page 9. In the next sections fabrication and characterization of DEP devices intended for sample pretreatment will be presented.

5.2 Design of DEP device

A simple DEP device concept used by many research groups consist of planar electrodes deposited and structured on a suitable substrate, with a fluidic system defined on top, see figure 5.1. By using glass substrates and by using SU-8 to define the fluidic system, a design very similar to the basic design of the presented PCR chip is obtained (see figure 2.1 on page 17). The only difference is that in the DEP structure the electrodes are not protected by a thin layer of SU-8. The DEP structures presented in this chapter are not only intended to test potential sample pretreatment functionality. There will also be structures to test general cell manipulation and characterization techniques.

Due to the similarity between the PCR chip design and the the DEP structure design monolithic integration of the two devices onto a single chip should be possible. The only obstacle can be the compatibility of the electrodes materials. Different requirements exist for electrodes used in DEP devices and electrodes used for heating and temperature sensing. In section 5.3 an evaluation of electrode materials will be given.

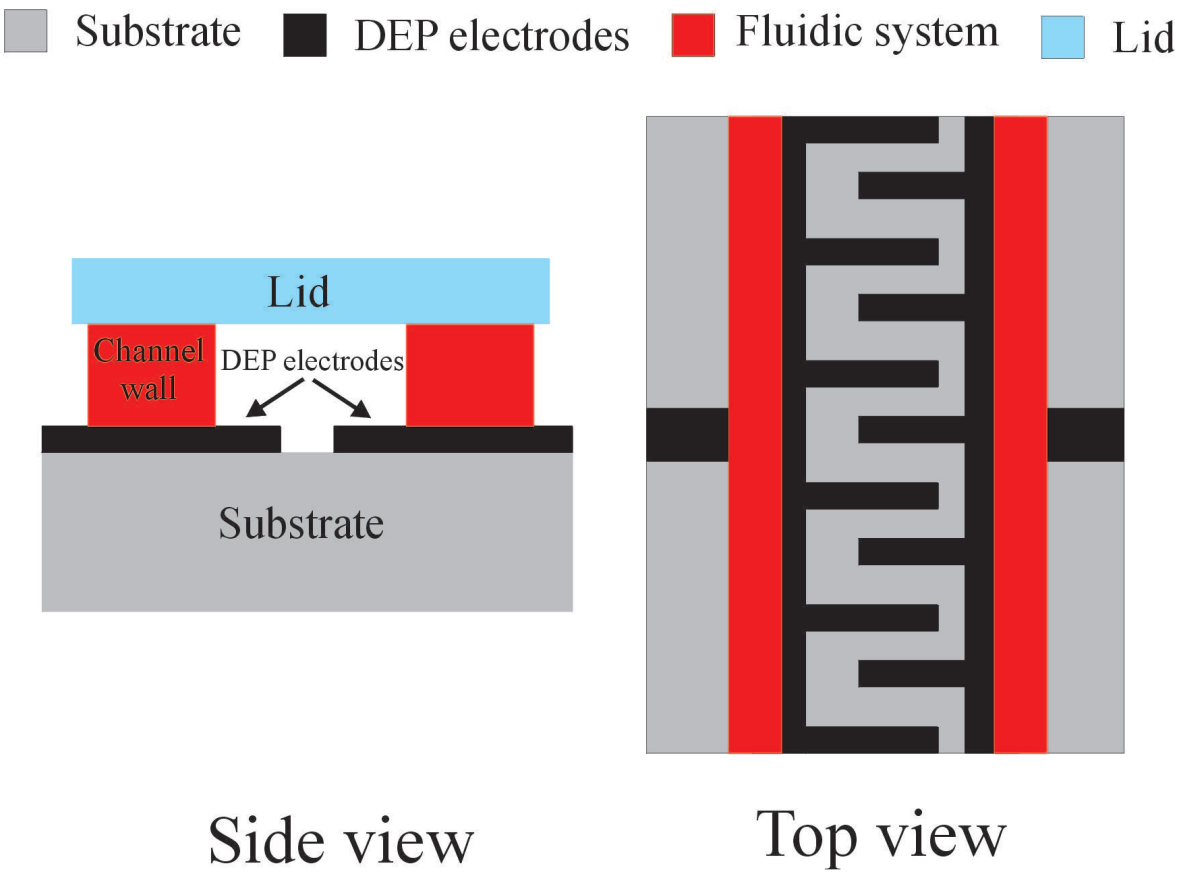

Figure 5.1: *Schematic of DEP design. DEP electrodes are fabricated on a substrate with a simple fluidic system on top. The fluidic system is sealed by a lid. The lid is omitted in the top view schematic for clarity.*

In order to test several different sample pretreatment techniques different electrode layouts have been used, and a few of them are shown in figure 5.2. Only one layer electrode structures have been designed for these test structures. Round spiral type travelling wave dielectrophoretic (TWD) structures like the one shown at the top right of figure 5.2 with 10μm and 5μm electrode size/spacing, as well as similar but square coil type TWD structures (not shown) with 10μm and 4μm electrode size/spacing are included. These structures were used to test TWD for cell manipulation and sample pretreatment. The advantage of the spiral and coil type TWD structures is that they can be implemented in a single electrode layer, unlike track type TWD structures that requires two electrode layers. Various castellated electrode designs, like the one shown in the top right of figure 5.2 as well as others, with electrode size/spacing of 4μm, 10μm and 20μm are also included. These structures were used to test the cell capture sample pretreatment technique. Finally the electroratation structures shown in the bottom left of figure 5.2 with opposite electrode spacing varying from approximately 10μm up to 25μm are included. The elctrorotation structures are only intended for cell characterization.

The fluidic system consists of a simple straight channel (see bottom right of figure 5.2) with a width of 400μm aligned to the center of the electrode structures. The task of the fluidic system is simply to move cells to and from the electrode structures.

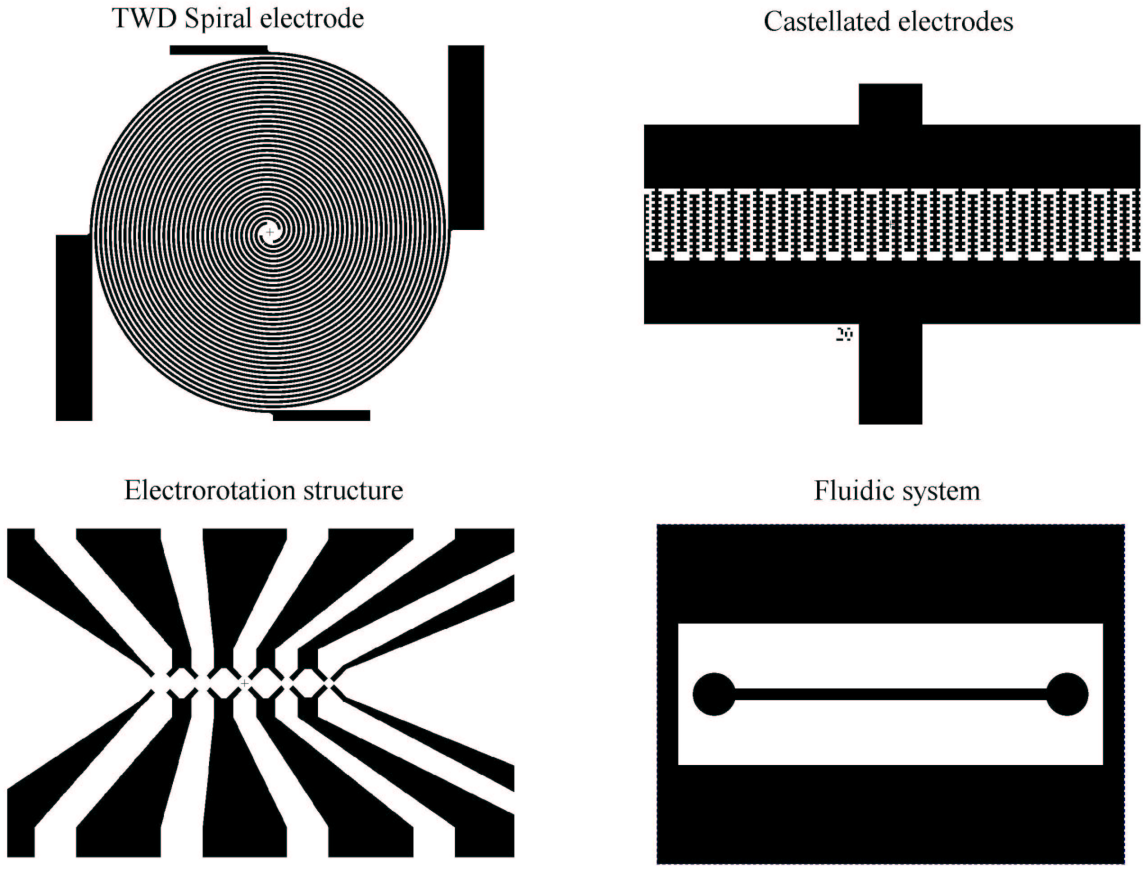

Figure 5.2: *Mask layout for DEP chip. 3 of the electrode structures included on the electrode mask are shown at the top and bottom left of the figure, spiral type TWD electrodes, castellated electrodes and electrodes for electrorotation, respectively. The mask at to the bottom right of the figure defines fluidic system. All masks are clear field masks.*

5.3 Electrode materials

The choice of electrode material for the DEP based sample pretreatment system is an important and difficult one. The electrodes must be able to function as DEP electrodes, which means that they must be able to operate in direct contact with electrolyte solutions with a wide range of conductivities. Furthermore, the type of sample pretreatment system possible with the DEP structures also depends on the material of the electrodes. TWD type devices are easiest implemented using two

layer electrodes, which requires an insulating layer between the electrodes. Such a layer is only available for some types of electrode materials at the process facility at MIC. Since the sample pretreatment system is intended to be monolithically integrated with the PCR chip presented in the previous chapters, process compatibility between the sample pretreatment system and the PCR chip is also needed. Based on these considerations and based on materials used in DEP devices presented in literature a number of electrode materials were evaluated.

5.3.1 Metal electrodes

Metal is the most widely used electrode material for DEP structures. Most of the presented structures in literature uses either gold [53, 55, 57, 58, 59, 60, 64, 93, 94, 95] or platinum [65, 64]. The advantages of gold or platinum electrodes is that it is a proven technique for DEP electrodes and they are also relatively easy to fabricate. Furthermore, platinum is the material used for the heater electrodes in the presented PCR chip and it is therefore an obvious candidate for electrode material in the sample pretreatment system. However, there are a number of disadvantages with respect to metal electrodes, some of them specific to the process facility at MIC. An inherent weakness of metal electrodes, is corrosion caused by electrolysis. This is especially a problem in high conductivity solutions and at low frequency [60]. A more specific limitation with gold or platinum metal electrodes is that neither gold or platinum are considered CMOS compatible and this limits the number of available processes at MIC. Two layer metal structures for TWD have been presented in literature using a nitride insulating layer [57, 60, 95] or a polyimide insulating layer [93], but neither layer is available for metal electrodes at MIC's process facility. In the LPCVD nitride process at MIC metals are not allowed, and at the time of this electrode evaluation there was no low temperature PECVD nitride process available. Thus use of two layer metal electrodes would require development of another type of insulating layer, compatible with the fabrication process for the PCR chip. Because of this two layer metal electrodes were dropped as a candidate for the electrode material in the sample pretreatment system.

Although 1 layer metal electrodes are still a viable option for the sample pretreatment system, alternative electrodes materials that are more corrosion resistant and where two layer electrodes are possible is preferred.

5.3.2 Silicide electrodes

As an alternative to metal electrodes silicides have been considered. Silicides are formed by solid-phase reaction of transition metals with silicon. Although not previously used in μTAS devices, silicides have found use as a low resistive and corrosion resistant material in the microelectronics industry [96, 97, 98, 99]. A large number of silicides can be formed, with nickel silicide (NiSi) and titanium silicide ($TiSi_2$) offering some of the lowest resistivities with 12-15$\mu\Omega$cm and 13-16$\mu\Omega$cm, respectively [98]. This is comparable with metal electrodes and makes nickel and titanium silicides useful as electrode material. Furthermore because silicides should be less prone to corrosion

they should able to function even at low frequency in high conductivity electrolytes. Nickel and titanium silicides thus have the potential to offer at least comparable and presumably better performance as electrode material than metals. However issues of compatibility both with respect to the integrated device as well as with the process equipment at MIC still needs to be considered.

Titanium silicide is formed at a relatively high temperature with the low resistivity phase requirering a temperature above 700°C. The advantage of this high temperature formation is that it gives titanium silicide good thermal stability which makes titanium silicide compatible with the nitride deposition processes available at MIC's process facility. Multilayer TWD electrodes can thus be fabricated using titanium silicide. 700°C is to high a temperature for the borosilicate glass substrate used in the presented PCR chip. However fused silica glass substrates can be used instead, although they are considerably more expensive than borosilicate substrates.

Nickel silicide can be formed at a relatively low temperature of 400°C or even lower [98, 99], making the silicidation process compatible with use of borosilicate substrates for the PCR chip. However nickel silicide is not compatible with the LPCVD nitride process, so when nickel silicide is used only one layer electrodes are possible.

Processing of silicide is slightly more difficult than metal electrodes. However, silicides were preferred over metal electrodes as the electrode material in the DEP based sample pretreatment system, because of the higher corrosion resistance. Both nickel silicide and titanium silicide electrodes will be used. However, emphasis was put on fabrication of titanium silicide electrodes due to the possibility of fabrication of two layer electrode structures.

5.3.3 ITO electrodes

Indium tin oxide (ITO) electrodes have a high optical transmission above 400 nm [100] and a relatively low resistivity, down to $\sim 200\mu\Omega$cm [101] and have mainly been used in the optoelectronics industry, i.e. in liquid crystal displays (LCD). Due to the advantages of optical transparency, ITO has also been used as electrode material in some 3D DEP devices [65, 66] where the electrodes otherwise would block the optical path.

ITO deposition is not available at the process facility at MIC and has not been considered for use in the sample pretreatment system. But because transparent electrodes can make observation of cells on top of electrodes easier, it was decided to test ITO for use in the DEP devices intended for characterization of various cell types.

5.4 Silicide DEP structures

Silicide was the material of choice for the DEP electrodes. The initial DEP structures for test of general cell manipulation and characterization techniques as well as for test

of potential sample pretreatment techniques prior to PCR, were fabricated with silicide electrodes on silicon substrates. Primarily titanium silicide structures, but also nickel silicide structures were fabricated and tested. After validation of the functionality of the silicide based DEP structures, it was tested if the structures could be fabricated on glass substrates, as this is necessary if the DEP structures are to be monolithically integrated with the PCR chip.

5.4.1 DEP silicide electrodes on silicon substrates

In this section the fabrication and characterization of titanium silicide and nickel silicide electrodes is presented. The fabrication process for the two materials is very similar and only slightly more complicated than fabrication of metal electrodes.

Fabrication of titanium silicide electrodes

Two fabrication methods were used in the processing of titanium silicide electrodes on silicon substrates, version A and version B. The fabrication sequence for the two methods is very similar as it is only the order of the process steps that differ, see figure 5.3. Only version B will be discussed in detail as this was the fabrication process used for all the titanium silicide DEP structures. The detailed process sequence for version B can be found in appendix C

First a 2μm LPCVD nitride layer is deposited on a silicon substrate. The nitride layer is used to insulate the electrodes from the substrate. The relatively thick layer is necessary to reduce capacitive coupling between the long spiral type TWD electrodes and the silicon substrate. On top of the nitride layer a 180nm LPCVD polysilicon layer is deposited as shown in figure 5.3.B1. It is in this layer that the silicide will formed.

1.5μm AZ5214E photoresist is spun onto the wafer and structured with the electrode mask using the image reversal process. 80nm titanium is deposited on the wafer using e-beam evaporation. A 30 second HF dip is applied just before the deposition of the metal to remove the natural oxide on the silicon. This is an important step as silicide formation is sensitive to the cleanliness of the metal/silicon interface [96]. The titanium is structured using a lift off process in an ultrasonic assisted acetone bath, figure 5.3.B2.

The silicide is formed using rapid thermal annealing (RTA) for 1 minute at a temperature above 700°C in an argon atmosphere, figure 5.3.B3.

The excess poly silicon not used to form the silicide structure is etched using a silicon reactive ion etch (RIE), figure 5.3.B4. The etching process is self-masking due to large selectivity between silicide etch rate and silicon etch rate. The etching of the polysilicon can also be done using potassium hydroxide (KOH).

Finally, any excess titanium that may not have reacted to form the silicide is removed in a piranha solution (4:1 H_2SO_4:H_2O_2), figure 5.3.B5.

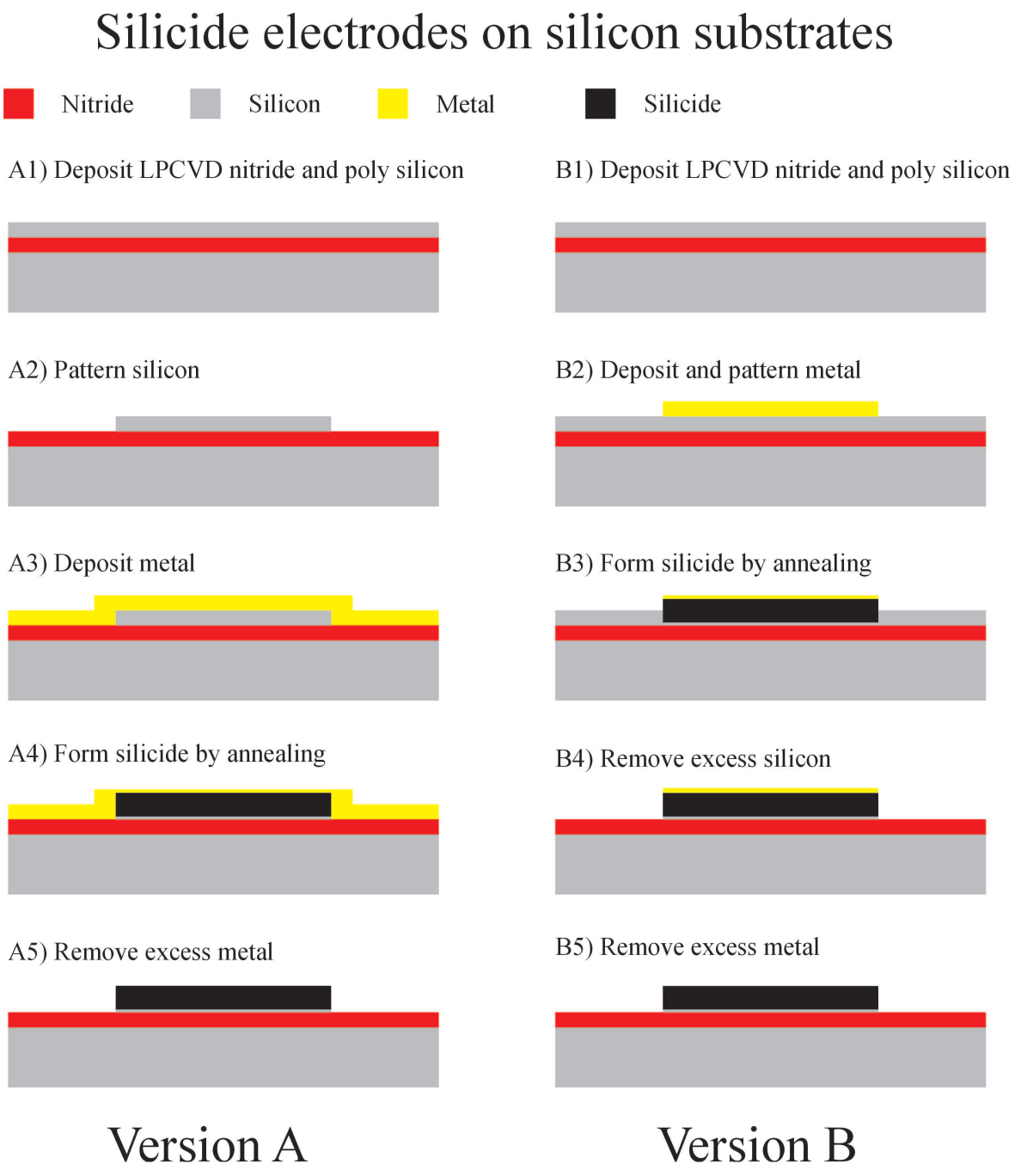

Figure 5.3: *Process sequence version A and version B for silicide electrode fabrication on silicon substrates. In version A the contact window for the silicide formation is defined by structuring the silicon layer. In version B the contact window is defined by patterning the metal layer.*

The main difference between version A and version B is that in version A the contact window (metal/silicon interface) for the silicide formation is defined by structuring the

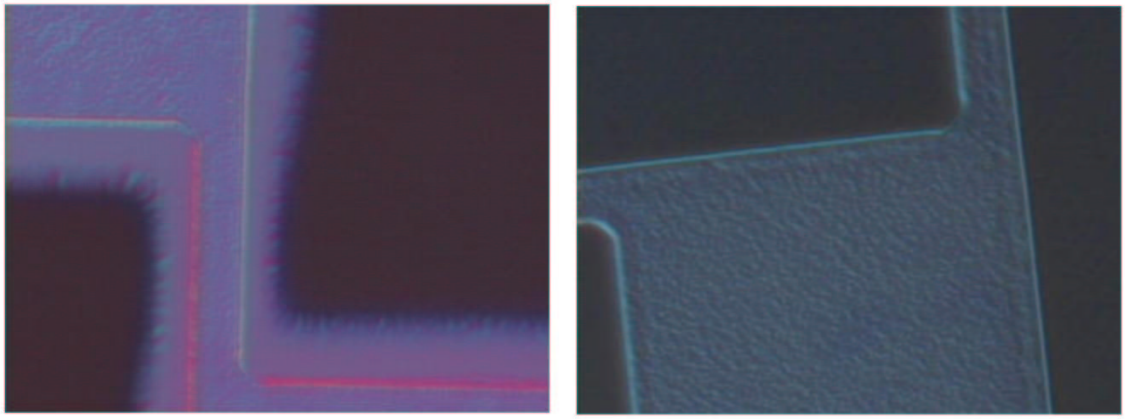

Figure 5.4: *Optical images of titanium silicide electrodes. In the image to the left version A of the fabrication process was used, while in the image to the right version B was used. The lateral definition of the structure fabricated using version A is very poor compared to the structure fabricated using version B.*

silicon layer. In version B the contact window is defined by patterning the metal layer. The reason for changing from version A of the process sequence to version B can be seen in figure 5.4. To the left is shown a titanium silicide structure fabricated using version A, while a silicide structure fabricated using version B is shown to the right. The lateral definition of the silicide structure fabricated using version A is very poor and not suitable to form microelectrodes. The reason for the poor lateral definition is that silicon is the dominant diffusing species during titanium silicide formation. Because of the metal covered sidewalls, see figure 5.3.A3, this leads to formation of silicide beyond the lateral dimensions of the contact window [96].

The formed silicide electrodes were characterized using secondary ion-mass spectroscopy (SIMS) and by electrical measurements. The SIMS measurements showed that the formed silicide had a thickness of approximately 160-170nm while the measured resistivity of the titanium silicide was $\sim 18\mu\Omega$cm, which is comparable to the values from literature [98]. Despite of the relatively thick nitride insulation layer it was found that RC coupling caused a significant decay in the amplitude of the applied signal towards the center of the spiral structures at medium to high frequencies [88].

Fabrication of nickel silicide electrodes

The fabrication of nickel silicide electrodes is similar to the fabrication of titanium silicide electrodes, the deposited metal is just nickel instead of titanium, see figure 5.3. The detailed process sequence can be found in appendix C. The silicide formation is done by annealing for 15 min at 425 °C. The removal of excess silicon is done using KOH, as nickel silicide is not RIE compatible at MIC. All nickel silicide structures

were formed using fabrication process version B. However as it is nickel that is the dominant diffusing species during the silicidation, version A should work to.

The formed nickel silicide electrodes were also characterized using SIMS and by electrical measurements. The SIMS measurements showed that the formed nickel silicide had a thickness of approximately 190nm while the measured resistivity of the titanium silicide was $\sim 20\mu\Omega$cm. This is slightly higher than the 12-15$\mu\Omega$cm found in literature [98]. The lateral definition of nickel silicide structures fabricated using process version B, was found to be comparable with the good lateral definition of the titanium silicide structures also fabricated using process version B.

5.4.2 Fabrication of silicide DEP devices

The fabrication of the DEP devices is a simple two mask process. First the silicide electrodes are fabricated and structured as described in the previous sections and using the electrode mask structures shown in figure 5.2. Most of the DEP devices have been made with titanium silicide electrodes, although nickels silicide electrodes have also been used.

The fluidic system is defined in SU-8. The wafers are dehydrated by baking in a 250°C oven for more than 3 hours prior to the spinning of SU-8. Immediately after the wafer has cooled a 75μm SU-8 (XP2075,Microchem) layer is spun onto the wafer with a rotation speed of 3000 rpm. The SU-8 layer is soft baked on a hotplate for 15 minutes at 95°C using a temperature ramp of 5 minutes to reach the bake temperature. After the bake the wafers are cooled by placing them on a non metallic surface, i.e. a stack of fab wipes. The chamber walls are defined by UV exposure through the mask that defines the fluidic system, see figure 5.2. The wafers are cross link baked for 20 minutes at 95°C using a temperature ramp of 5 minutes to reach the bake temperature. Then the wafers are cooled on the hotplate until room temperature is reached. Finally, the SU-8 is developed in PGMEA for approximately 10 minutes and the DEP device chips have been realized. The detailed process sequence can be found in appendix C.

In figure 5.5 left is shown a SEM micrograph of a castellated 10μm electrode structure prior to the definition of the fluidic system. To the right is shown an optical image of a 10μm spiral electrode TWD structure with the SU-8 fluidic system defined on top.

5.4.3 Packaging

A schematic of the DEP device packaging method is shown in figure 5.6. The packaging method is very similar to the chip carrier packaging presented for the PCR chip in section 3.4. A PDMS bonded lid is used to seal the fluidic system and wire bonding is used for the electrical interconnects. However with DEP chip packaging, fluidic interconnects have been drilled through the chip and chip carrier. The advantage of this packaging method is that optical access through the lid is possible using microscope objectives. Adhesive bonding of the lid with glue have also been utilized.

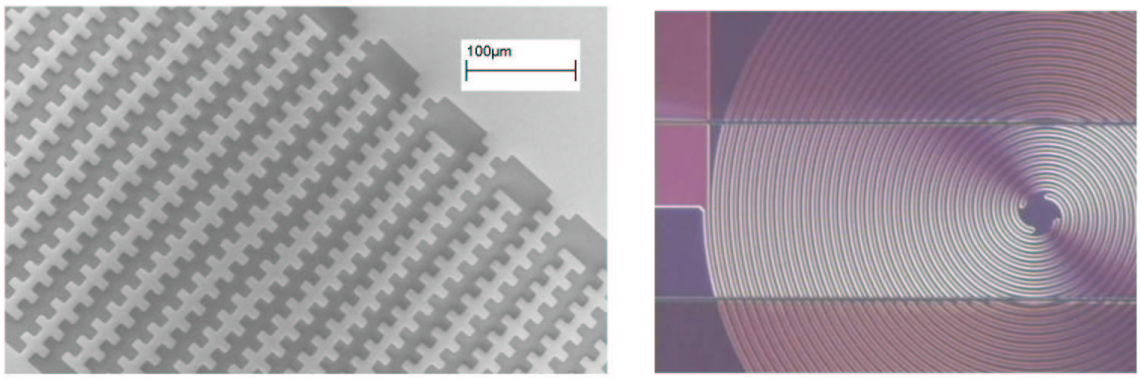

Figure 5.5: *To the right of the figure is shown a SEM micrograph of a castellated 10µm electrode. To the left is shown an optical image of a 10µm spiral TWD structure with the SU-8 fluidic system defined on top.*

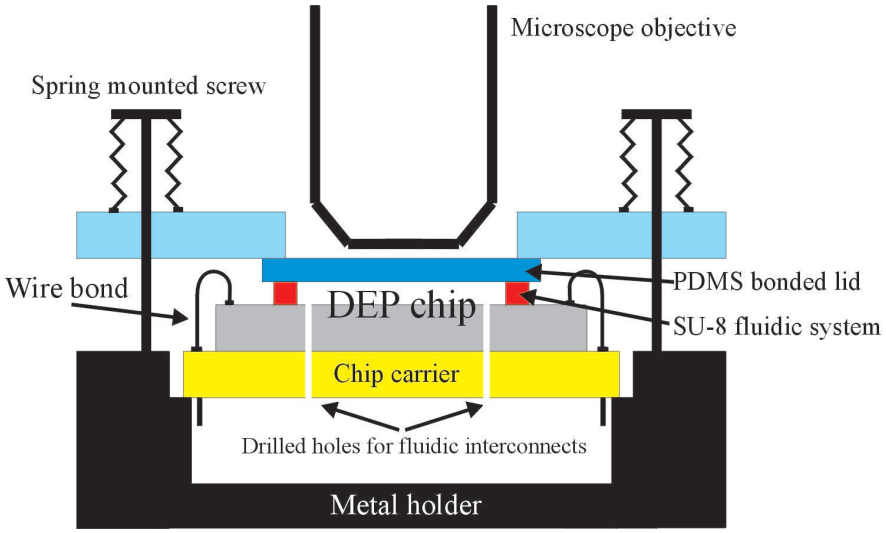

Figure 5.6: *Schematic of DEP chip packaging. The DEP chip is packaged using a ceramic chip carrier. Electrical interconnects are made with wirebonding, while holes are drilled through chip and carrier for the fluidics connection. A PDMS bonded lid is used to seal the fluidic system. The DEP structures can be observed through a microscope objective.*

5.4.4 Cell characterization, manipulation and sample pretreatment by DEP

In this section validation of the functionality of the DEP devices will be presented. Cell manipulation and potential sample pretreatment techniques were tested on yeast cells and with campylobacter and E-coli bacteria. More results and detailed information about experimental conditions can be found in [88, 102].

One of the potential advantages expected from use of silicide instead of metal electrodes is increased corrosion resistance. The silicide electrodes showed no sign of degradation even in experiments at very low frequency in electrolyte solutions where boiling of the liquid occurred.

Figure 5.7 shows a yeast cell in an electrorotaton device. The rotating electrical field induces a torque on the cell and the cell rotates. The rotation velocity is a measure of the polarisability α_i (see equation 5.1-2) and these kinds of experiments can thus be used to characterize different types of cells and find the frequency range of p-DEP and n-DEP. This can provide valuable information about the sample pretreatment techniques that can be applied.

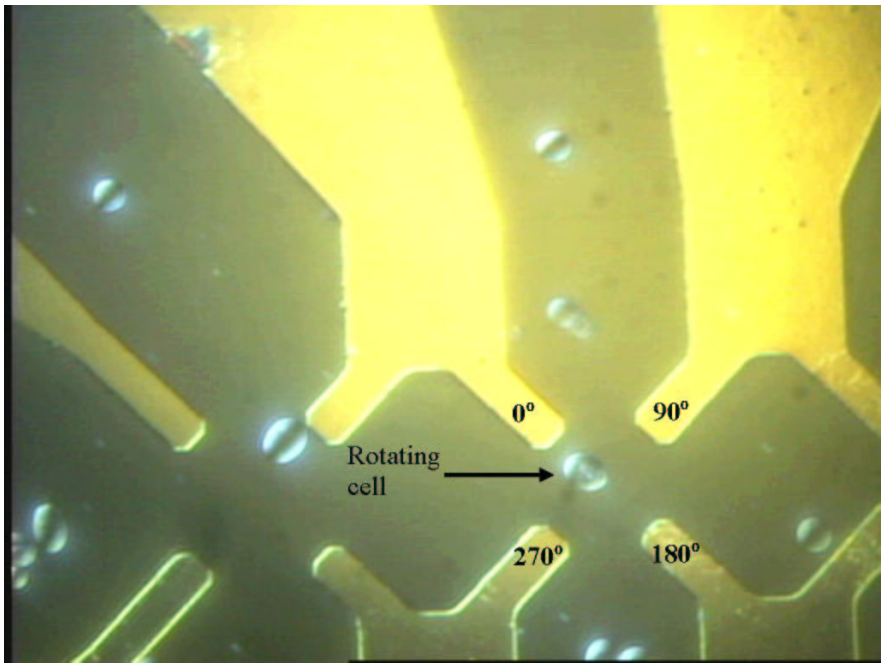

Figure 5.7: *Optical image of a yeast cell in an electrorotation device. A rotating field is generated by connecting the electrodes to four 90° phase shifted signals.*

In figure 5.8 is shown a test of the cell capture technique. Yeast cells flowing across one of the castellated electrode structures are captured and immobilized by p-DEP at frequencies of the applied signal above ∼350kHz in a solution with a conductivity of ∼30μS/cm. At relatively low flow velocity the capture efficiency approaches 100% until the electrode array is completely filled with several layers of cells. As can be seen in the figure the electrodes are darkened by the layers of yeast cell. The thickness of the layer depend on the amplitude of the applied signal. The cell capture technique is thus able to provide up-concentration of the sample. However, upon release some degree of dilution of the cells occurs due to the parabolic flow profile.

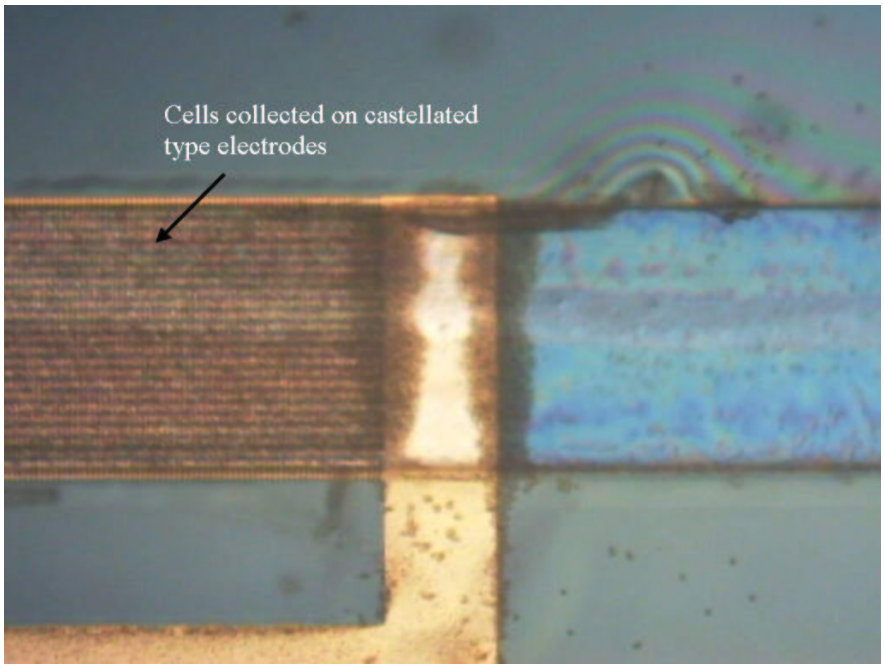

Figure 5.8: *Optical image of yeast cells captured with a castellated electrode device. Cells flowing across the electrodes are immobilized under the influence of p-DEP. Several layers of cells can be captured by the electrodes.*

In equation 5.1-1 describing the DEP force it can be seen that the effective polarisability α_r of the particle relative to the surrounding media depends on the conductivity σ_m of the media. As the conductivity σ_m of the media increases $\alpha_r \rightarrow -0.5$. Particles will thus be under the influence of n-DEP in media with very high conductivity and can not be captures by the DEP electrodes. Experiments with increasing media conductivity shows that cells will only be immobilized on the electrodes if the conductivity of the media is below 500-1000μS/cm. Thus the cell capture devices will only work with samples where the conductivity is below 500-1000μS/cm.

In figure 5.9 is shown a fairly advanced sample pretreatment technique using coil type TWD structures involving both up-concentration and separation of non-viable and viable yeast cells mixed in a solution with a conductivity of $\sim 30\mu$S/cm. The non-viable yeast cells have been dyed dark blue using methylene blue. At a frequency of 4MHz the non-viable cells under the influence of n-DEP and TWD force are collected, and thus concentrated at the center of the structure, see top left of figure 5.9. The viable cells are under the influence of p-DEP at this frequency and therefore captured at the electrodes. By reversing the order of the phase at the four electrodes the TWD force is directed outwards and the non-viable yeast cells transported towards the edge of the electrode structure (see top right of figure 5.9), where they are collected. By changing the frequency of the applied field to 50kHz the viable yeast cells now under the influence

of n-DEP and TWD are collected and up-concentrated at the center of the structure, see bottom left of figure 5.9. By changing the phase of the applied signal they are now also transported toward the edge of the electrode structure, bottom right of figure 5.9. It is seen that a few viable and non-viable cells continues to be captured at the electrodes. Compared to the cell capture technique above where the captured cells are moved afterwards by a fluidic flow, there is less dilution of the concentrated cells during TWD transportation resulting in a more confined sample after the DEP treatment.

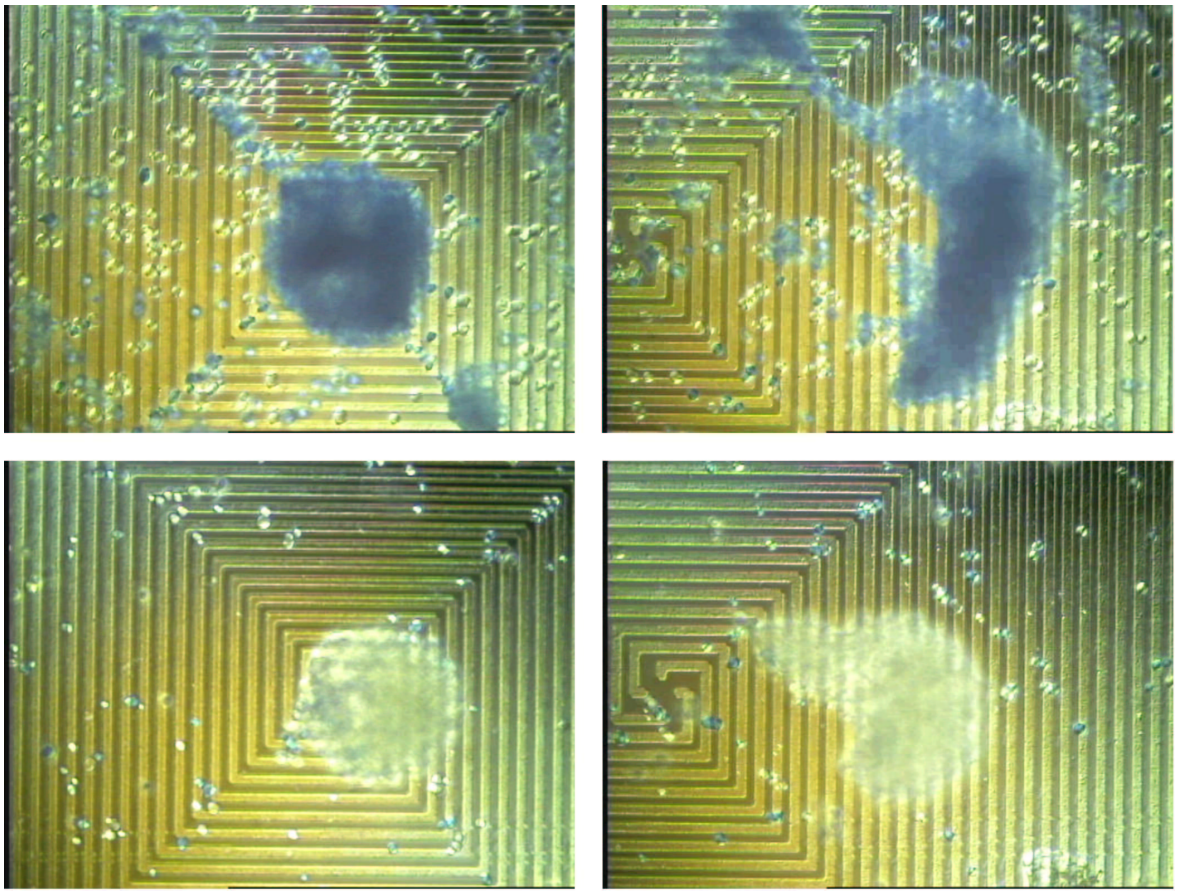

Figure 5.9: *Optical images of TWD cell up-concentration and separation of viable (clear) yeast cells and non-viable (blue) yeast cells. At the top of the figure, non-viable yeast is up-concentrated and transported under the influence of n-DEP and TWD, with viable cells immobilized at the electrodes by p-DEP. At the bottom of the figure, the viable yeast is up-concentrated and transported under the influence of n-DEP and TWD.*

In all the examples shown here the observation of the cells is done with a camera through a microscope objective. In chapter 9 a method to integrate planar waveguides for optical detection compatible with the fabrication of the DEP chips is presented.

The DEP devices have also been tested with E-coli and campylobacter bacteria. However, observation and thus also photographic reproduction of small bacteria is very difficult. In this case use of transparent ITO electrodes manufactured on glass substrate could help to improve the observation.

The simple cell manipulation and characterization experiments show that DEP devices with silicide electrodes have the potential to provide advanced sample pretreatment functionality prior to PCR.

5.5 DEP Silicide electrodes on glass substrates

If the DEP structures are to be integrated on chip with the PCR chip, they have to be fabricated on glass substrates. In this section the fabrication of titanium silicide on fused silica substrates and the fabrication of nickel silicide on Borofloat and fused silica substrates is presented.

5.5.1 Silicides on glass

Glass substrates in this thesis can be either borosilicate substrates or fused silica substrates. The fused silica used (Hoya Corporation, 4W55-325 STD [103]) is a clean high temperature stable glass and is therefore compatible with both LPCVD and RIE processes at MIC. The borosilicate glass used (Borofloat, Schott corporation [84]) on the other hand is only stable below ∼500°C [84] and is also considered an impure glass and is thus not allowed in the LPCVD and RIE processes at MIC. Figure 5.10 shows a general fabrication procedure for silicides on glass wafers. It is very similar to version B of the fabrication process for silicide on silicon wafers, shown in figure 5.3 on page 66. However, depending on whether borosilicate or fused silica glass substrates is used, the actual fabrication steps can differ.

5.5.2 Titanium silicide electrodes on fused silica

Because the fabrication of titanium silicide requires an annealing temperature above 700°C only fused silica substrates can be used. The initial fabrication procedure uses the same process parameters as the titanium silicide fabrication on silicon substrates presented in section 5.4.1. The detailed process sequence can be found in appendix C

4 inch fused silica substrates from Hoya corporation [103] is used as substrate. The wafers are cleaned in a piranha (4:1 H_2SO_4:H_2O_2) and rinsed in water. A 180nm LPCVD polysilicon layer is deposited as shown in figure 5.10.1. This layer will be used to form the silicide.

1.5μm AZ5214E photoresist is spun onto the wafer and structured with the electrode mask using the image reversal process. 80nm titanium is deposited on the wafer using

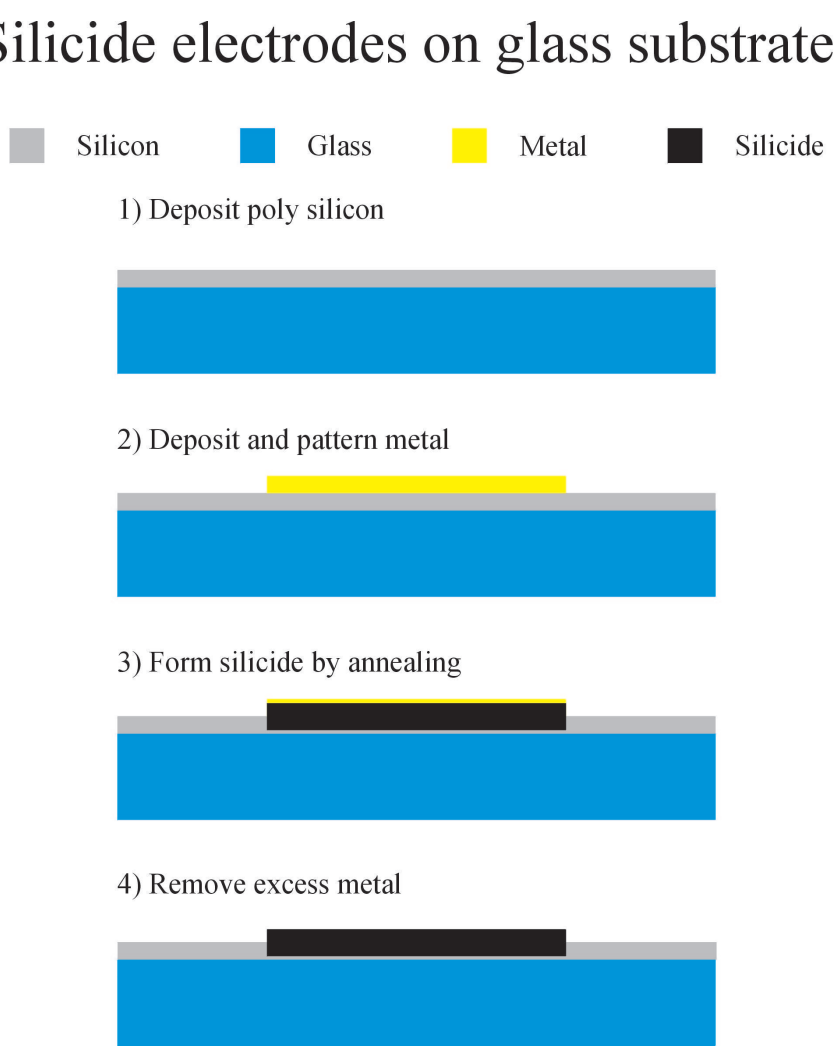

Figure 5.10: *Process sequence for silicide electrode fabrication on glass substrates.*

e-beam evaporation. A 30 second HF dip is applied just before the deposition of the metal to remove the natural oxide on the silicon. The titanium is structured using a lift off process in an ultrasonic assisted acetone bath, figure 5.10.2.

The silicide is formed using Rapid Thermal Annealing (RTA) for 1 minute at a temperature above 700°C in an argon atmosphere, figure 5.10 3).

Finally, any excess titanium that may not have reacted to form the silicide is removed in a piranha solution (4:1 H_2SO_4:H_2O_2), figure 5.10.4.

Although the similar fabrication procedure on silicon substrates resulted in high quality silicide as shown in the previous sections, the quality of the silicide on fused silica is very bad. To the left in figure 5.11 is shown an optical image of typical formed silicide. The silicide is full of cracks and is furthermore not electrically conductive. The crack-

ing is due to very high tensile stress in the silicide layer. Silicides in general have a coefficient of thermal expansion (CTE) that is significantly higher than that of silicon which has a CTE of $\sim 2.6 * 10^{-6}/°C$ [104]. Therefore a high level of tensile stress is in general present in silicide films [96]. Titanium silicide has a CTE of $\sim 12.5 * 10^{-6}/°C$ [105, 106]. Fused silica has a CTE of $\sim 0.5 * 10^{-6}/°C$ [107], which is even lower than silicon. Therefore the level of tensile stress in a silicide film on fused silica is very high. Furthermore, there is also tensile stress in the LPCVD polysilicon layer, used to form the silicide, when deposited on fused silica substrates and the combined effects has caused the titanium silicide to crack.

In order to minimize the tensile stress in the silicide film a thinner silicide can be used. Using a process identical to the above, but using a 100nm polysilicon layer and a 35nm titanium layer instead a thinner silicide is formed, see appendix C for detailed process sequence. An optical image of the thinner silicide on fused silica can be seen to the right in figure 5.11. The electrode has a width of 4μm and the quality of the silicide is good in most areas. However in some places the silicide film has flaked off due to poor adhesion to the substrate and the stress in the layer. This poor adhesion is probably due to a non-clean metal-silicon interface at these positions prior to the silicidation. Thin silicide films are more sensitive to the cleanliness of the interface than thicker films. Electrical characterization of the silicide gives a thickness of the thinner titanium silicide of $\sim$ 50nm which is less than a third of the titanium silicide used on silicon substrates. Attempts to make the silicide on fused silica slightly thicker results in formation of cracks and high resistance of the film.

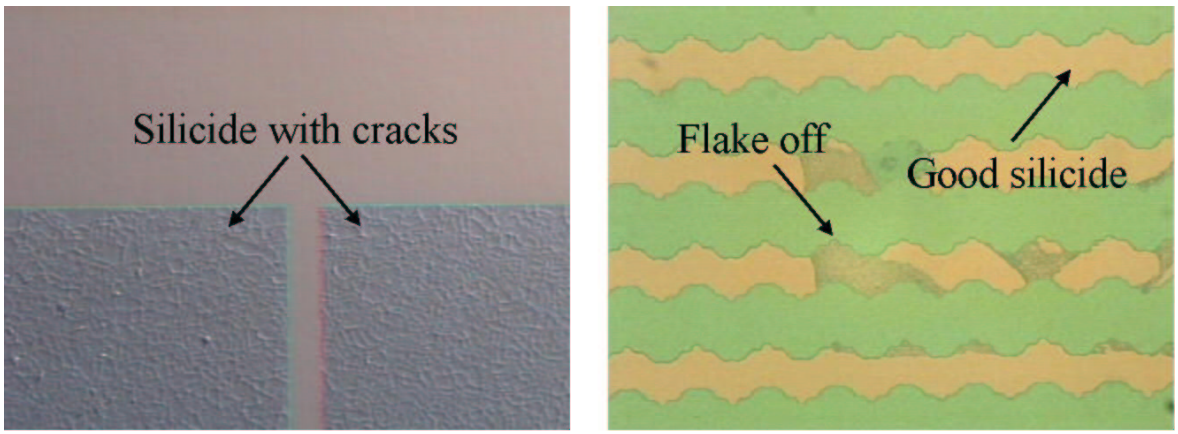

Figure 5.11: *Optical images of titanium silicide structures on fused silica substrates. The image to the left shows a thick silicide electrode while the image to the right shows a thin silicide electrode. The thick silicide is full of cracks due to stress in the layer. The thin silicide looks good in most places, but in some areas there is flaking, again due to stress in the layer.*

The thin titanium silicide electrodes are not resistant enough to endure either a KOH or a RIE etch for removal of the excess silicon as done in the silicide electrodes on

silicon substrates. This is why these steps have been omitted. The electrodes are also too fragile to be coated with LPCVD nitride with subsequent RIE etch of contact holes. So while 2 layer electrode structures with titanium silicide can be done on silicon substrates, it is not possible on the fused silica substrates. Track type TWD structures for sample pretreatment can thus not be integrated with the PCR chip, as titanium silicide is the only readily available electrode material for two layer electrode structures at MIC.

5.5.3 Nickel silicide on glass substrates

Compared to titanium silicide, nickel silicide has the advantage that is is formed at a lower temperature (425°C) than titanium silicide (above 700°C). The stress in the nickel silicide films due to the mismatch in the CTE should thus be smaller. Furthermore nickel silicide can also be formed on Borofloat wafers, due to the relatively low formation temperature. Borofloat glass has a CTE of $\sim 3.25 * 10^{-6}/°C$ [84] which is comparable with that of silicon. Therefore the tensile stress in the nickel silicide film on Borofloat wafers should be comparable with that of nickel silicide films on silicon wafers, which did not show any signs of stress induced cracking.

The nickel silicide fabrication on fused silica is identical to the thin titanium silicide process, but with nickel as metal instead of titanium (see figure 5.10) and with silicide formation by annealing for 15 minutes at 425°C. Because of the expected lower stress in the nickel silicide film, a thicker film should be possible and a metal layer of 60nm is used instead of the 35nm used for the titanium silicide. The detailed process sequence can be found in appendix C.

An optical image of nickel silicide electrodes on fused silica is shown in the left side of figure 5.12. The image is taken with bottom illumination and the nickel silicide structures are the dark areas. No sign of flaking is observed even though the thickness of the silicide film is approximately 110nm according to electrical measurements, more than double the thickness of the thin titanium silicide films on fused silica.

Borofloat substrates are not compatible with LPCVD processes due to the low temperature stability. The fabrication of nickel silicide electrodes on Borofloat substrates is therefore slightly different than on fused silica. A 100nm sputtered silicon layer is used instead of the LPCVD silicon layer. Besides this the fabrication is identical to the fabrication on fused silica. The detailed process sequence can be found in appendix C.

An optical image of nickel silicide on Borofloat glass is shown to the right in figure 5.12. No flaking of nickel silicide film is observed, and the electrical properties of the film are similar to the nickel silicide films on fused silica substrates.

No efforts have been made to increase the thicknesses of the nickel silicide on the glass substrates. It should be possible to achieve similar silicide thickness on Borofloat glass substrates as with silicon due to the similar CTE of the two materials.

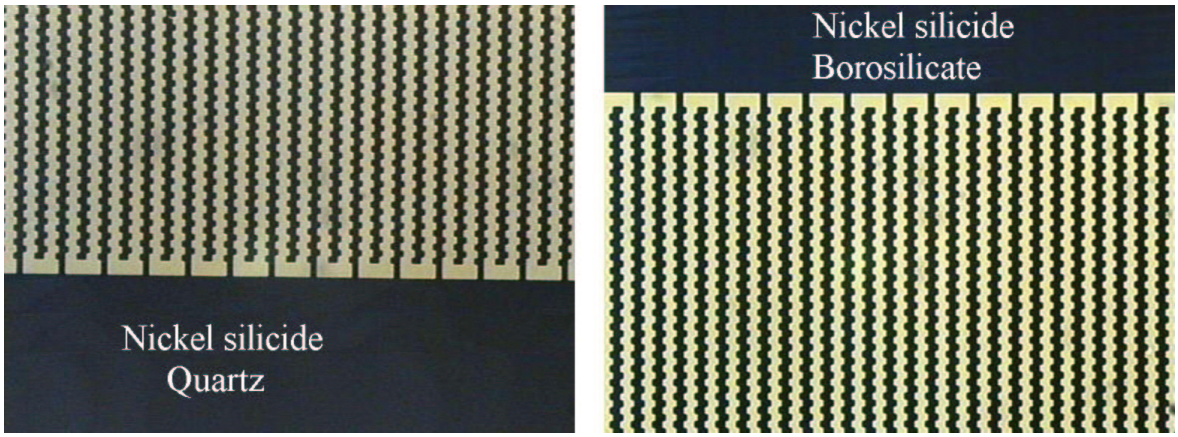

Figure 5.12: *Optical images of nickel silicide electrodes on fused silica substrates (to the left) and Borosilicate substrates (to the right). On both types of substrates the quality of the nickel silicide looks good, with no signs of cracking or flaking.*

The performance of nickel silicide electrodes on glass substrates is significantly better than that of titanium silicide on fused silica and approaches that of silicide on silicon substrates. Because of process compatibility issues two layer nickel silicide electrodes are not possible. However all the single layer electrode structures used to test the cell manipulation and potential sample pretreatment techniques can also be fabricated with nickel silicide electrodes on both fused silica and on Borofloat substrates. The use of nickel silicide electrodes thus makes on chip integration of DEP based sample pretreatment structures with the presented PCR chip possible.

5.6 ITO electrode structures

Due to the potential advantage of transparent electrodes, indium tin oxide (ITO) electrodes were also investigated. ITO based DEP structure were intended only for use in cell manipulation and characterization devices. They were to be used in cases where observation of cells could prove difficult, i.e. with very small cells and bacteria. Process compatibility with the presented PCR chip therefore does not play a role in these devices. However, to get an advantage from the transparency of the electrodes, only glass substrates can be used for the ITO structures. Borofloat wafers with 300 nm of ITO deposited at Central Research Laboratories [108] were used for the DEP devices.

ITO can be structured using plasma etching [109], laser ablation [65, 66] and by wet etching in acidic solutions [110, 111, 112, 100]. Structuring by wet etching is the only method available at the process facility at MIC. Unfortunately wet etching of ITO is known to be difficult as the etching behavior is dependant on deposition conditions, annealing treatments and also the etch solution [100, 110, 112, 100]. Inhomogeneity in the micro-crystallinity of the films can lead to etch rates ranging from very high

to very low, resulting in poor linewidth control, accelerated under-etching and etch residues. The structuring experiments were carried out using a 6M HCL etch solution and using photoresist as etch mask.

All the potential difficulties with wet etching of ITO were encountered. Etching of the 300 nm ITO layer took anywhere from $\sim$ 30 seconds to 10 minutes, varying both with position on the wafer and from batch to batch. This resulted in either large mask undercut and/or etch residues.

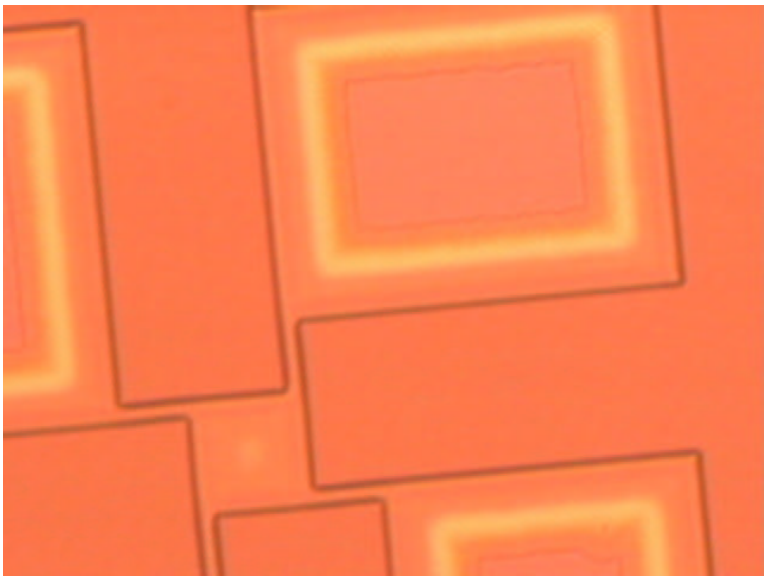

Figure 5.13: *Optical image of ITO electrode structure with resist mask on top. After severe mask undercutting during the wet etching of the ITO, only the large areas of the intended structure is left. All the smaller features are completely removed.*

In figure 5.13 an optical image of an ITO electrode structure with resist mask on top is shown. There is severe undercutting of the resist mask, so all the small linewidth features are completely removed.

In figure 5.14 some of the best results with structuring of the ITO is shown. To the left is shown a castellated structure with 20μm feature sizes on the lithography mask, while the structure to the right is a spiral type TWD structure with 5μm linewidth on the lithography mask. In this case the mask undercutting was to a few μm. However, at other places on the wafer there were problems with etch residues.

It is known that annealing of ITO can improve the homogeneity of the microcrystalline structure, resulting in more uniform etching [110, 111, 100]. However attempts to anneal the ITO films resulted in an increase of the resistivity, from the already relatively high $\sim$ 600$\mu\Omega$cm for the as deposited films, up to more than 1000$\mu\Omega$cm for the annealed films.

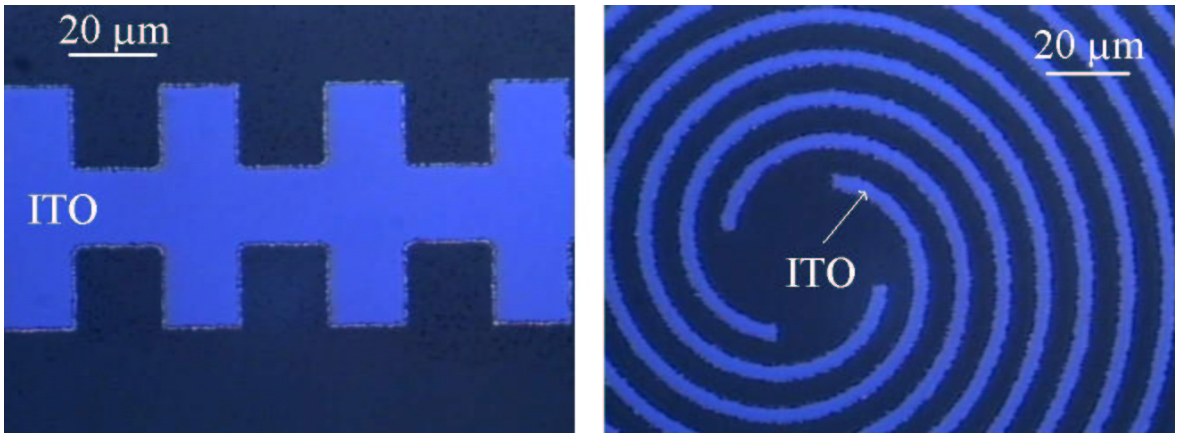

Figure 5.14: *Optical images of ITO electrodes structured by wet etching. To the left a 20µm castellated electrode and to the right a 5µm spiral type TWD electrode. The electrode edges are quite rough but there is only a mask undercutting of a few µm.*

Due to these difficulties it was judged that the advantages that could potentially be gained from the transparency of ITO electrodes were not worth further efforts, and work with ITO based DEP structures was abandoned.

5.7 Summary

In this chapter design, fabrication and test of DEP based devices for cell manipulation and sample pretreatment have been presented. Titanium silicide and nickel silicide were chosen as electrode material for the DEP structures due to high corrosion resistance and, in the case of titanium silicide, the potential for two layer electrode structures. Test devices on silicon substrates validated the cell manipulation and sample pretreatment functionality for one layer electrode structures. Fabrication on glass substrates caused problems for titanium silicide due to stress induced cracking and flaking. This prevents potential realization of two layer electrode structures on glass substrates. One layer nickel silicide structures on glass substrates however showed similar performance as the silicide electrodes on silicon substrates. It can therefore be used to integrate DEP based sample pretreatment systems with the presented PCR chip. ITO was investigated for transparent electrodes, but work was abandoned due to difficulties with the etching process.

Chapter 6

Design of PCR chip with integrated sample pretreatment

In this chapter design of a PCR chip with integrated DEP based sample pretreatment is presented. The device is based on the PCR chip design presented in chapter 2 and the DEP devices presented in chapter 5. The two components are fabricated on a glass substrate and are connected by a fluidic system. Compatibility issues between the sample pretreatment system and the PCR chip will be discussed and based on these considerations the fluidic system connecting the two will be presented. Thermal and fluidic simulations will be used to model the expected performance of the integrated PCR chip.

6.1 Design

The basic design idea for the PCR chip with integrated DEP based sample pretreatment is shown in figure 6.1. The design is based on the PCR chip presented in chapter 2 and the DEP based sample pretreatment systems presented in chapter 5. The integrated chip is realized on a glass substrate. The sample pretreatment system is based on nickel silicide DEP electrode structures, while the SU-8 based PCR chamber has integrated thin film heaters and a temperature sensor to control the PCR thermocycling. A fluidic system connects the sample pretreatment system with the PCR chamber.

In the next sections the design of the three main components of the chip are presented: The DEP based sample pretreatment system, the PCR chip and the fluidic system connecting the two.

6.1.1 The DEP based sample pretreatment system

In chapter 5 a variety of different DEP based cell manipulation and sample pretreatment techniques were presented. The sample pretreatment system used in the integrated design is based on these devices. The presented DEP devices used silicide DEP electrodes. Due to fabrication issues only single layer nickel electrode structures can

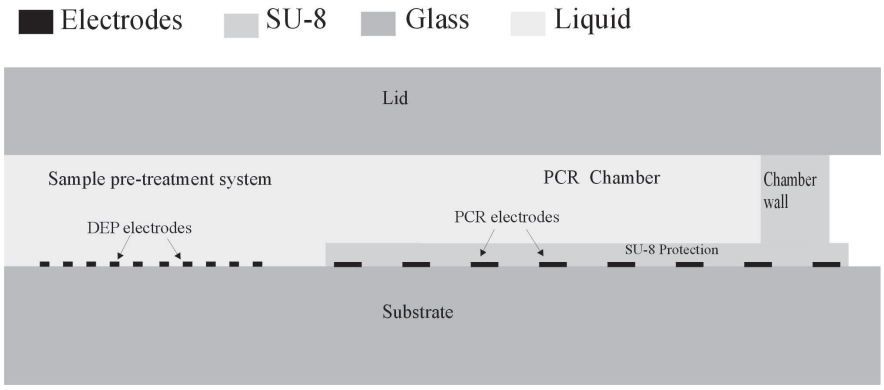

Figure 6.1: *Schematic of envisioned design for integration of PCR with sample pre-treatment. A DEP based sample pre-treatment system is integrated on chip with a SU-8 based PCR chip fabricated on a glass substrate. The chip integrates thin film electrodes to control the PCR thermocycling.*

be fabricated on glass substrates. The sample pretreatment system is thus limited to DEP functionalities that can be implemented using a single electrode layer.

For the DEP based sample pretreatment system on the integrated PCR chip, a cell capture device is used (see sections 1.2.1 and 5.4.4). Although TWD devices can be implemented in a single electrode layer, and can perform advanced sample pretreatment, like separation and concentration of cells (see section 5.4.4), the cell capture technique was preferred due to the simpler operation of such devices.

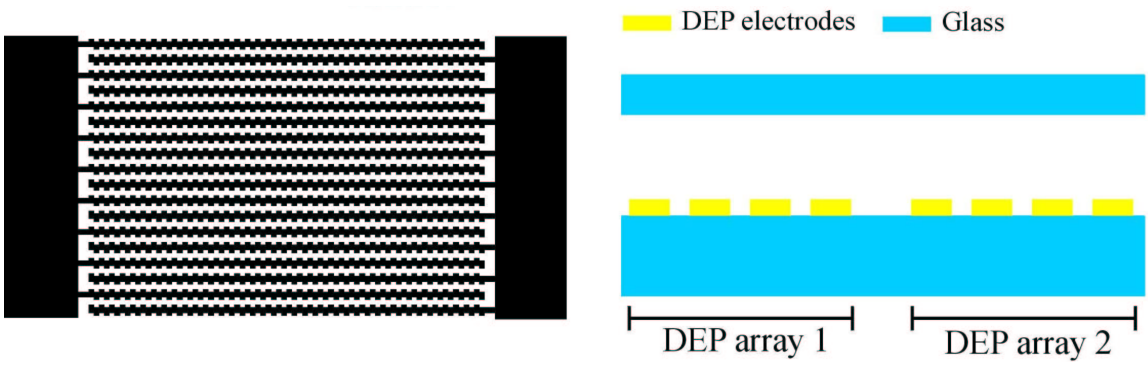

Figure 6.2: *To the left in the figure: Castellated DEP electrode array with electrode size/spacing of 10μm. To the right in the figure: Schematic of the DEP based sample pretreatment system. The DEP electrodes are fabricated on a glass substrate with a fluidic system on top. Two independent arrays of the castellated DEP electrodes are used in the system.*

Figure 6.2 to the left shows part of an electrode array with the castellated electrode geometry that is used for the DEP electrodes. The electrode size/spacing is 10μm. A schematic of the sample pretreatment system is shown to the right in figure 6.2. The DEP electrodes are fabricated on the glass substrate with a fluidic system on top. The device is sealed by a PDMS bonded lid. Two separate DEP electrode arrays are used in the sample pretreatment system. The electrode arrays can be operated at different frequencies.

In the cell capture method the wanted cells are captured by p-DEP at the electrode edges, while unwanted components are removed using liquid flow. This is done by choosing a frequency of the applied electrical field where the wanted cells experience p-DEP and the unwanted components experience n-DEP. By using two electrode arrays that can operate at different frequencies, cell types that does not experience p-DEP at the same frequency can be collected simultaneously. Figure 6.3 shows a schematic of sample pretreatment using the cell capture technique, with the two electrode arrays operating at different frequencies. First the two wanted cell types are captured under the influence of p-DEP at the electrode edges in the two electrode arrays, while a third unwanted component, under the influence of n-DEP, is only weakly bound in regions of low field gradient, figure 6.3.1. Then the unwanted component is washed out of the sample, figure 6.3.2. Finally the collected cells can be released and transported to the PCR chamber, figure 6.3.3. This is done by flowing an appropriate liquid through the system as will be discussed in more details later.

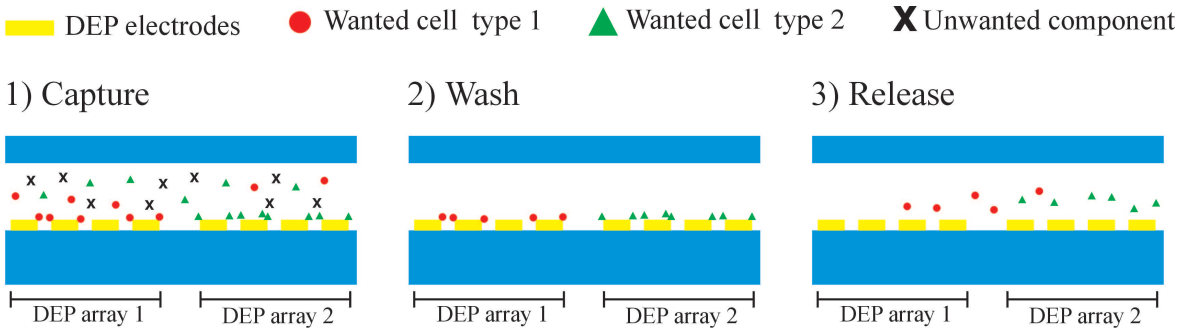

Figure 6.3: *Schematic of the cell capture sample pretreatment technique. 1) Wanted cells are immobilized under the influence of p-DEP at the electrode arrays. 2) Unwanted components are then washed out of the sample. 3) Finally the collected cells can be released and transported with the flow to the PCR chamber.*

In most cases it is of interest to collect only one cell type in the sample pretreatment system. Thus in many cases the challenge in a DEP based sample pretreatment system is to find a frequency where only the wanted cell type experiences p-DEP, while all other components experience n-DEP or at least negligible p-DEP.

6.1.2 The PCR chip

The PCR chip on the integrated design is essentially a smaller version of the PCR chip presented in chapter 2, see figure 2.12 on page 32. The PCR chamber is made smaller so that the die size of the PCR chip with integrated sample pretreatment system is small enough to fit the ceramic chip carrier used in the packaging of the device (MCPG14434, 0.7" die attach size, Spectrum Semiconductor materials [87]). In the integrated design the PCR chamber size is reduced to ~10μL. The heater electrodes extend 700μm beyond the inside of the PCR chamber wall like in the previously presented PCR chip. This is done to minimize cold wall effects. A schematic of the PCR design is shown in figure 6.4

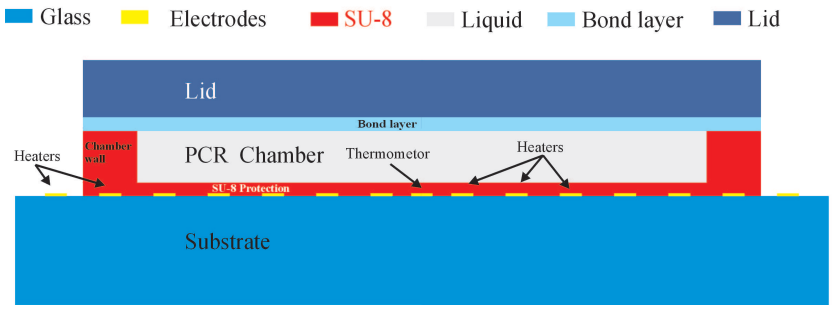

Figure 6.4: *Schematic of PCR design in the integrated chip. A 10μL PCR chamber is fabricated on a glass substrate. A resistive thermometer is placed in the center of the PCR chamber with heater arrays for the PCR thermocycling positioned on each side. The heater spacing in the arrays are 100μm and the heaters extend beyond the chamber walls to minimize cold wall effect. The PCR electrodes are protected by a thin layer of SU-8. The lid material can be either polymer or glass.*

The PCR chamber is fabricated on a glass substrate, either a 1000μm borosilicate substrate or a 500μm fused silica substeate. The PCR chamber is 400μm high and has an area of 5000μm x 5000μm. The SU-8 PCR chamber wall has a width of 400μm. The heater structure consist of a total of 64 heaters in two heater arrays with 32 heaters with a width of 20μm and a length of 6400μm in each of the arrays. The spacing between heaters in an array is 100μm. The two heater arrays are placed symmetrically on each side of a resistive thermometer that is positioned in the bottom center of the PCR chamber. The resistive thermometer has a width of 20μm and a length of 4920μm and is connected using 4-terminal connections. The two heater arrays are positioned so the heater spacing at the position of the thermometer is 100μm as in the rest of the PCR chamber. The heaters and the thermometer are protected from PCR buffer with a 5μm SU-8 layer. The lid can be either a polymer or a glass lid and is bonded using a reversible PDMS bond.

6.1.3 Compatibility issues with PCR and DEP

The compatibility consideration discussed in the previous chapters have been purely fabrication related. The presented PCR chip and DEP based cell handling systems have been designed in such a way that they can readily be integrated in a single device without compatibility issues in the fabrication process. However, fluidic consideration with respect to the properties of the aqueous media in which PCR and DEP is performed also needs to be considered.

In section 5.1 we found that for a spherical particle with absolute permittivity ε_p^* and radius r suspended in a medium with absolute permittivity ε_m^* the DEP force is given by equation 6.1-1.

$$F_{DEP} = 2\pi r^3 \varepsilon_m \alpha_r \nabla E^2 \quad , \text{ where } \alpha_r = Re\left[\frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*}\right] \text{ with } \varepsilon_i^* = \varepsilon_i + \frac{\sigma_i}{j\omega} \quad (6.1\text{-}1)$$

ε_i is the permittivity and σ_i is the conductivity of the particle or the surrounding media. α_r is the real part of the Clausius-Mossotti factor and defines the effective polarisability of the particle relative to the surrounding media. $\alpha_r > 0$ for p-DEP and $\alpha_r < 0$ for n-DEP. As the conductivity σ_m of the media increases $\alpha_r \rightarrow -0.5$. Particles will thus be under the influence of n-DEP in media with very high conductivity, and will not be captured by the DEP electrodes.

In experiments with the DEP capture devices presented in chapter 5 it has been found that cells would only be immobilized by the electrodes if the conductivity of the media is below 500-1000μS/cm. This sets a limit for the type of samples that can be used in the sample pretreatment system. They have to have a conductivity below 500-1000μS/cm.

PCR is performed using so called mastermix solutions. A PCR mastermix consist of several components including primers, polymerase, deoxynucleotides (the four bases in DNA) and water containing ions that is used to optimize the PCR reaction. The DNA to be amplified, template DNA, is added to the PCR mastermix. The template DNA is extracted from the sample in form of whole cells by the sample pretreatment system in the integrated PCR chip. However, PCR mastermix is an optimized solution and the contents must not change radically with the addition of the template DNA.

The typical conductivity in a PCR mastermix is more than a magnitude higher than the maximum conductivity that can be used in the sample pretreatment system. The sample pretreatment thus needs to be performed in a separate medium than the PCR amplification. After this, the cells must be transported to the PCR chamber and mixed with the PCR mastermix but without changing the content of the mastermix radically. This involves quite a lot of fluidic handling, and the fluidic system used to perform these tasks is presented in the next section.

6.1.4 The fluidic system

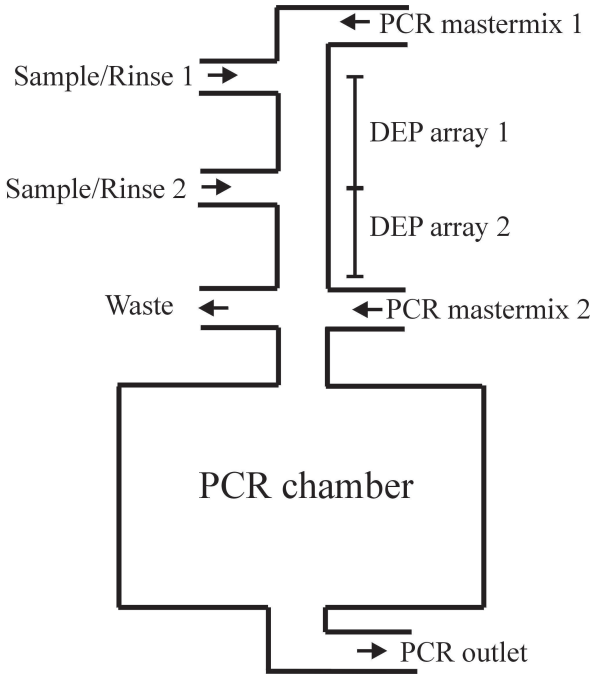

Figure 6.5: *Schematic of the fluidic system used in the integrated PCR chip. A network of 400μm wide channels connects the sample pretreatment system (the two DEP arrays) with the PCR chamber. The system has a total of 6 inlets/outlets, of which 4 is intended as inlets while the remaining two are intended as outlets. The inlets/outlets are named in the figure according to the intended functionality during operation of the device.*

In order to perform the sample pretreatment, transport the treated sample in form of whole cells to the PCR chamber and mix the sample with the PCR mastermix, a quite complicated fluidic system is used. A schematic of the fluidic system is shown in figure 6.5. The fluidic system uses a network of 400μm wide channels to connect sample pretreatment system and PCR chamber with each other and with inlets and outlets. The system has a total of 6 inlets/outlets, of which 4 is intended as inlets while the remaining two are intended as outlets. Of the inlets, the two inlets denoted sample 1 and sample 2 are intended for sample input to the pretreatment system at the two DEP electrode arrays. This is where the wanted cells are captured, see figure 6.3.1. One or both of these inlets are also used during the washing step in the sample pretreatment system, see figure 6.3.2. Waste from the sample pretreatment system is collected through the outlet denoted waste. The inlet denoted PCR mastermix 2 is intended to use for filling of the PCR chamber with PCR mastermix, while the inlet, PCR mastermix 1, is used to transport the sample into the PCR chamber after the sample pretreatment, see figure 6.3.3. This transportation is done using PCR mastermix to minimize the change of the mastermix content in the PCR chamber during addition of the sample. The PCR amplicon is collected at the second outlet denoted PCR outlet.

Figure 6.6 shows a schematic of how sample pretreatment with subsequent transportation of the sample to the PCR chamber can be done using the fluidic system. In figure 6.6.1, the samples is introduced trough the two sample inlets. The wanted cells are collected at the DEP electrodes, while unwanted components continues through the sample pretreatment system and out through the waste. The PCR chamber is constantly filled with PCR mastermix to keep the untreated sample out. In figure 6.6.2 rinsing solution (typically water) is introduced trough the two sample/rinse inlets to wash the remaining unwanted components in the sample out through the waste. Finally the treated sample is transported into the PCR chamber by introducing PCR mastermix through inlet 1, see figure 6.6.3. During this step there will be some dilution of the mastermix in the PCR chamber, but due to the large volume ration between the camber and the rest of the fluidic system, the dilution should be minimal.

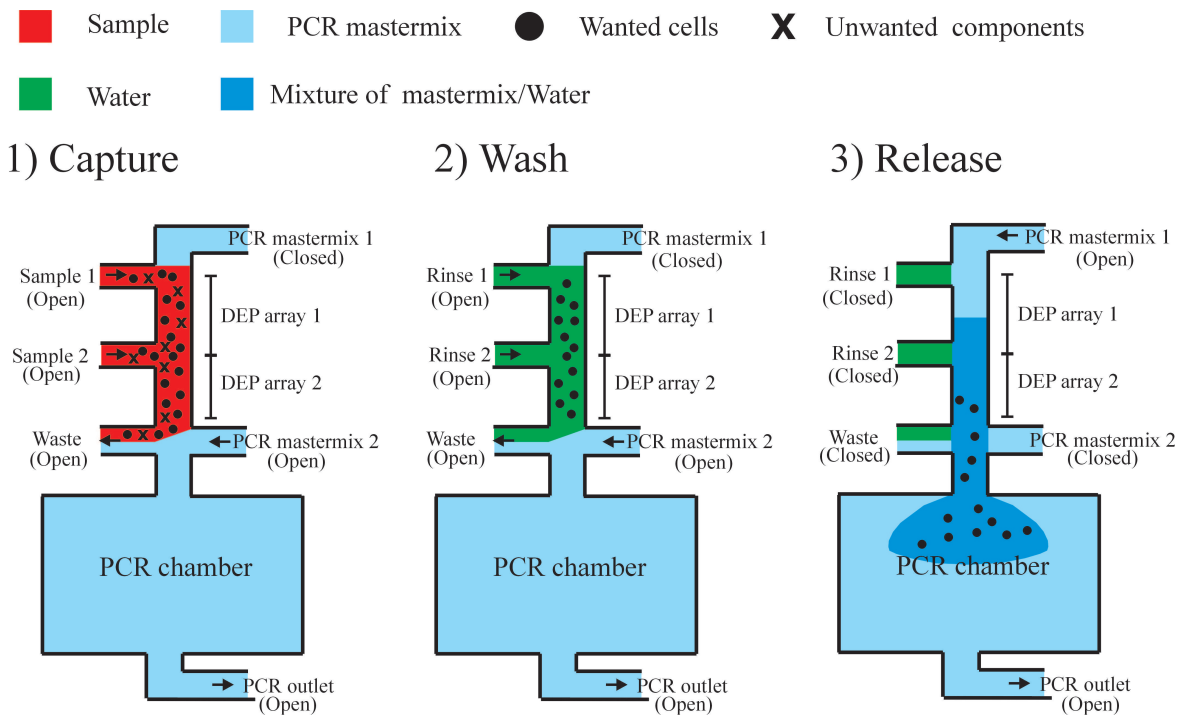

Figure 6.6: *Schematical example of sample pretreatment. 1) Sample is flown through the sample pretreatment system and wanted cells are captured by the DEP electrode arrays. Simultaneously, the PCR chamber is constantly filled with PCR mastermix to keep untreated sample out. 2) Unwanted components remaining in the sample pretreatment system is washed out by flowing rinsing solution through the system. 3) The captured cells are released and transported to the PCR chamber using a flow of PCR mastermix. During this step there will be some dilution of the mastermix in the PCR chamber.*

PCR mastermix is relatively expensive and during real operation of the sample pretreatment system in the integrated PCR chip one would normally not have a constant

flow of mastermix to fill the PCR chamber and keep untreated sample out as in the schematic presented in figure 6.6. This can just as well be done with water and then switching to PCR mastermix just before the sample release step. There are of cause many possible combinations of fluidic handling in a system with 6 inlet/outlets and the above is only one suggestion.

To evaluate the performance aspects of the chosen fluidic system 3D CFD-ACE simulations of the flow in both the channel part and the chamber part of the fluidic system is used. The simulations are presented in section 6.3.

6.1.5 Final design

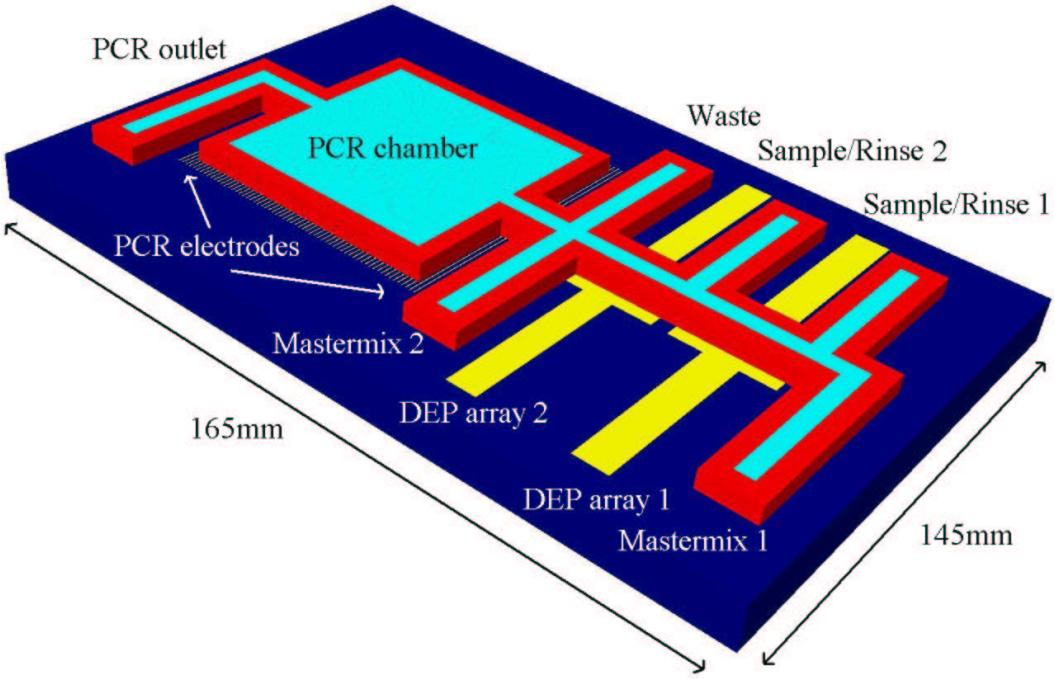

Figure 6.7: *Schematic of the final design of PCR chip integrated with DEP based sample pretreatment system. The total chip size is 165mm X 145mm. Half of the chip is used for the sample pretreatment system, the other half for PCR. The two system is connected by a fluidic system.*

Figure 6.7 shows a schematic of the final design for the PCR chip with integrated DEP sample pretreatment system. The total chip size is 165mm X 145mm so the chip can be packaged using the ceramic chip carriers used previous for the DEP devices, see section 5.4.3 on page 68, and the PCR chip, see section 3.4.2 on page 46. The sample pretreatment system takes up about half the space, with the PCR chamber taking up the other half. The two systems are connected using the fluidic system presented in figure 6.5.

6.2 Thermal simulations

The PCR functionally of the integrated chip is based on the PCR chip presented in chapter 2. Although a different size PCR chamber is used, most of the thermal performance characteristics presented for the PCR chip in section 2.3 also apply for the integrated design. However, the integrated designs includes a fluidic system connected to the PCR chamber and the influence this has on the temperature homogeneity needs to be investigated. Further more the integrated design will be realized on both a 1000μm borosilicate substrate, like the previous presented PCR chip, as well as on a 500μm fused silica substrate. The influence of the thinner fused silica substrates on the power consumption and the cooling rate, also needs to be investigated.

The thermal properties of the integrated chip are modelled using the equivalent circuit representation of the 1D model presented in section 2.3.2 and section 2.3.3 and using a modified version of the 3D CFD-ACE FEM model presented in section 2.3.7. In the modified version version of the CFD-ACE model a fluidic system leading to the PCR chamber has been included.

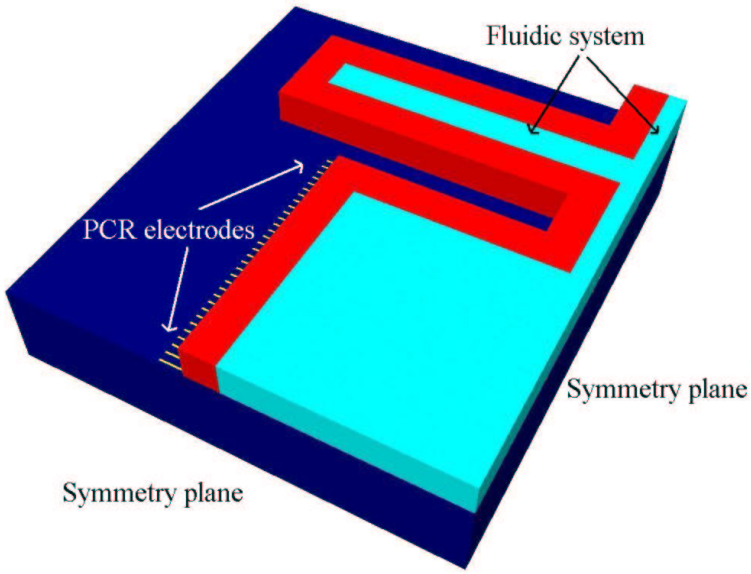

Figure 6.8: *Schematic of 3D CFD-ACE FEM model of integrated PCR chip. The lid has been omitted for clarity. The model has been implemented to scale, except for the heaters, which for meshing purposes have been modelled as being 2 μm high. 2-fold symmetry has been applied to the model to reduce computing requirements. The position of the thermometer in the model is on the top of the substrate along the left symmetry plane of the model.*

The same model assumptions used in the thermal models presented in chapter 2, see section 2.3.1 on page 19, have also been used in the thermal modelling of the integrated design. Thus the PCR electrode protection layer, the bond layer for the lid and the effects from the packaging of the chips are not included in the modelling.

A schematic of the 3D CFD-ACE model of the integrated chips is shown in figure 6.8. In the figure the lid has been omitted for clarity. The 3D model is build using the CFD-ACE micromesh model generator. A convection boundary condition is applied to the lid and other free surfaces of the device. To model the heatsink an isothermal boundary condition is applied to the bottom of the substrate. As previously, the heaters are not implemented to scale due to meshing considerations. The heaters are modelled as being 2μm high. Besides this and the model assumptions stated above, the model is implemented with the geometry described in section 6.1.2.

A heated area of 6400μm x 6400μm, which is the area spanned by the heaters in the design has been assumed in the 1D SPICE model, so that the power consumption can be compared with the 3D CFD-ACE model. For both models the target temperature of the PCR chamber is 94°C.

6.2.1 Temperature homogeneity

As mentioned previously the temperature distribution in the PCR chamber needs to be relatively homogeneous. In the PCR chip design presented in chapter 2, which is the design the integrated PCR chip is based on, the temperature distribution in the chamber was fairly homogeneous except for a small temperature drop near the edge of the chamber (see figure 2.13 on page 34). However, in the integrated design a fluidic system connects cold areas of the chip with the PCR chamber. Further more, as the lid also extends to seal the colder parts of the device, the properties of the lid can also influence the temperature uniformity in the PCR chamber. To see the effect of this, 3D CFD-ACE simulations of the temperature distribution in the PCR chamber and in the connected fluidic system is used. The simulations are made using both a 500μm glass lid as well as for a 500μm polymer lid.

Figure 6.9 shows a CFD-ACE simulation of the temperature distribution in the PCR chamber and the fluidic system leading to the chamber, for a target temperature of 94°C in the PCR chamber. This simulation is with a 500μm glass lid. The simulation shows that the influence of the fluidic system connecting the PCR chamber with colder parts of the chip is minimal. As for the PCR chip the design is based on, a homogeneous temperature distribution in the PCR chamber is predicted with a small temperature drop near the edges. Only regions of the lid at or near the PCR chamber is heated to a temperature close to the target temperature of 94°C. However, there are regions of elevated temperature extending several mm away from the PCR chamber. To the right in the figure a view plane with a cut through the center of the chamber and fluidic system is shown. It is seen that the elevated temperature region also extends some distance distance into the fluidic system.

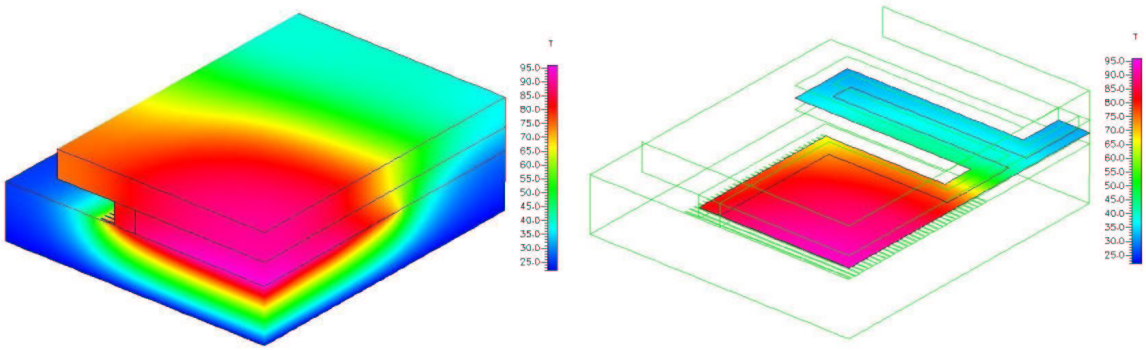

Figure 6.9: *3D CFD-ACE simulation of the temperature distribution in integrated design using a glass lid. A target temperature of 94°C in the PCR chamber is used. To the left a general view of the simulation is shown, to the right a view plane cut parallel to the substrate half way up in the chamber is shown. The temperature distribution in the PCR chamber is homogeneous, but with a small temperature drop near the edges. Regions of elevated temperature extend several mm away from the position of the PCR chamber.*

Figure 6.10 shows a simulation of the temperature distribution when a polymer lid is used. The temperature distribution in the PCR chamber is almost identical to the simulation using a glass lid (figure 6.9). A homogeneous temperature distribution in the chamber is obtained, but with a small temperature drop near the edges. However, the regions of elevated temperatures of the lid and in the fluidic system are more confined than when a glass lid is used.

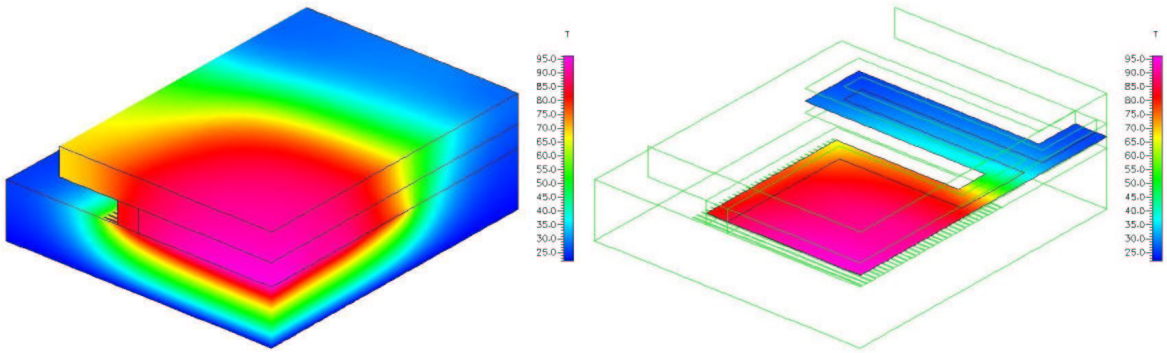

Figure 6.10: *3D CFD-ACE simulation of the temperature distribution in integrated design using a polymer lid. A target temperature of 94°C in the PCR chamber is used. To the left a general view of the simulation is shown, to the right a view plane cut parallel to the substrate half way up in the chamber is shown. The regions of elevated temperature are almost completely confined to the area of the PCR chamber.*

6.2.2 Power consumption

We know from the previous presented PCR chip, that the power consumption of the PCR chip design is very dependent on the substrate thickness (see figure 2.6 on page 26). The integrated PCR chip will be realized using both a 1000μm borosilicate substrate and a 500μm fused silica substrate. The thermal conductivity of fused silica is slightly higher than that of borosilicate, see table 2.2 on page 21, so it can be expected that the power consumption of the chip using fused silica substrates is relatively high. Table 6.1 shows the predicted power consumption of the integrated PCR chip found by the 1D model and the 3D CFD-ACE model for both a 1000μm borosilicate substrate and a 500μm fused silica substrate. The target temperature for the PCR chamber is 94°C in both models.

Table 6.1: *Simulated power consumption for integrated PCR chip at 94°C*

Simulation model		1D	3D CFD-ACE
1000μm Borosilicate:	Power consumption @ 94°C [w]	3.2	3.4
500μm fused silica:	Power consumption @ 94°C [w]	8.2	7.8

The 1D models predict a power consumption of 8.2W for the 500μm fused silica substrate and 3.2W for the 1000μm borosilicate substrate. The 3D CFD-ACE model predicts a power consumption of 8.2W for the 500μm fused silica substrate and 3.4W for the 1000μm borosilicate substrate. The expected slower decrease in power consumption with increasing substrate thickness for the 3D model compared to the 1D model is thus also observed for the integrated PCR chip (see section 2.3.6 on page 27). The power consumption when a 500μm fused silica substrate is used is relatively high. However, because of the smaller PCR chamber in the integrated PCR chip design, the power consumption on the 1000μm borosilicate substrate is smaller than for the PCR chip presented in chapter 2, 3.4W vs. 5.7W, respectively. This correspond to the difference in the area spanned by the heaters in the two designs, 6400μm x 6400μm and 8200 x 8200μm, respectively.

6.2.3 Cooling rates

Like the power consumption, the cooling rates are also very substrate dependant. However, with the chamber size and substrate thicknesses used, the cooling rates are almost independent of the actual size of the PCR chamber. Thus the cooling rate for the integrated PCR chip on 1000μm borosilicate substrates is identical to the cooling rates found for the previous presented PCR chip in section 2.5.4, which is also realized on 1000μm borosilicate substrates.

We know from the previous presented PCR chip that the cooling rate is very large for thin substrates. This caused problems for the 2D ANSYS FEM model used. Thus the cooling rates for the integrated PCR chip on 500μm have only been modelled using 3D CFD-ACE simulations and the 1D SPICE simulations.

Figure 6.11 shows the CFD-ACE and SPICE simulations of an integrated PCR chip on a 500μm fused silica substrate for the temperature transition from 94°C to 60°C. This corresponds to the typical cooling step during the PCR cycle from the denaturation temperature (94°C) to annealing temperature (60°C). The temperature transition is modelled in the center of the PCR chamber at the position of the thermometer. The SPICE simulations are for both a 500μm glass lid and for a 500μm polymer lid. The CFD-ACE simulation is with a 500μm glass lid.

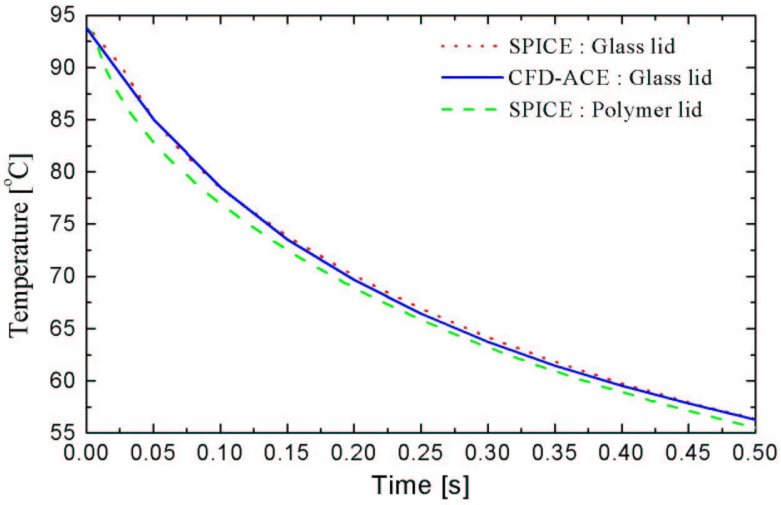

Figure 6.11: *1D SPICE and 3D CFD-ACE simulations of the temperature drop from 94°C when the power to the heaters are turned off at time t=0. The simulation is for a 500μm fused silica substrate and both polymer and glass lids are used. The temperature drops slightly faster when a polymer lid is used according to the 1D SPICE model, especially in the at the beginning of the cooling step.*

Both the the 1D SPICE model and the 3D CFD-ACE model predicts an average cooling rate between 90°C and 80°C of ∼150°C/s when a glass lid is used. The temperature drops slightly faster when a polymer lid is used according to the 1D SPICE model, especially in the at the beginning of the cooling step. However, as was also found previously, at later times the influence of the lid configuration diminishes and the cooling rates begin to approach each other. For both a polymer lid and a glass lid the SPICE model predicts an average cooling rate of ∼85°C/s, for the temperature transition from 90°C to 60°C. The same values are found for the CFD-ACE model with a glass lid.

The predicted cooling rates at the position of the thermometer, for both a 1000μm borosilicate substrate and 500μm fused silica substrate, when glass lids are used, is summarized in table 6.2.

Table 6.2: *Simulated cooling rates of integrated PCR chip at position of thermometer*

Simulation model		1D SPICE	3D CFD-ACE
1000μm borosilicate	: Average cooling rate 90°C → 80°C [°C/s]	∼40	∼40
1000μm borosilicate	: Average cooling rate 90°C → 60°C [°C/s]	∼20	∼20
500μm fused silica	: Average cooling rate 90°C → 80°C [°C/s]	∼ 150	∼ 150
500μm fused silica	: Average cooling rate 90°C → 60°C [°C/s]	∼85	∼85

As expected from the previous presented chip, the cooling rates in the integrated PCR chips are very high when a 500μm fused silica substrate is used. The cooling rates are more than 3 times larger than when a 1000μm borosilicate substrate is used. However, it has to be remembered, the cooling rates are dependent on the position in the PCR chamber, as found previously. At the top of the PCR chamber the temperature transitions are much slower. Table 6.3 shows the predicted cooling rates at the top of the chamber by SPICE simulations, for both a 500μm fused silica substrate and a 1000μm borosilicate substrate. The cooling rate at the top of the chamber when using a 500μm fused silica substrate is larger than for a 1000μm borosilicate substrate, but only with a factor of two.

Table 6.3: *Simulated cooling rates of integrated PCR chip at the top of the chamber*

Substrate	Temperature transition	Average cooling rate [°C/s]
1000μm borosilicate	: 90°C → 80°C	∼12
1000μm borosilicate	: 90°C → 60°C	∼10
500μm fused silica	: 90°C → 80°C	∼ 24
500μm fused silica	: 90°C → 60°C	∼22

The predicted thermal performance of the integrated PCR chip is very similar to the previously presented PCR chip, which the integrated chip is based on. Due to the smaller chamber size, the power consumption is lower than for the previous presented chip when 1000μm borosilicate substrates are used. However, when the integrated chips uses a 500μm fused silica substrate the power consumption increases with more than a factor of two. Even though the lid and the fluidic system connects colder areas of the chip with the chamber, the temperature homogeneity in the PCR chamber is still relatively uniform. When a 500μm fused silica substrate is used, the cooling rates increases with at least a factor of two compared to 1000μm borosilicate substrates, depending on the position in the PCR chamber.

6.3 Fluidic simulations

The sample is transported from the sample pretreatment system into the PCR chamber using the fluidic system presented in section 6.1.4. The laminar flow conditions

typically present in microfluidic systems has some consequences for the sample transport from the sample pretreatment system into the PCR chamber. In order to evaluate the influence of the flow behavior on the sample transport, 3D CFD-ACE simulations have been used. The model used includes the PCR chamber as well as the adjacent flow channels leading into and out of the PCR chamber.

6.3.1 Flow in the sample pretreatment system

The sample pretreatment part of the fluidic system consist of 400μm wide and 400μm high flowchannels. Figure 6.12 shows a simulation of the flow velocity in the channels for a total volumetric flow of 40μL/min.

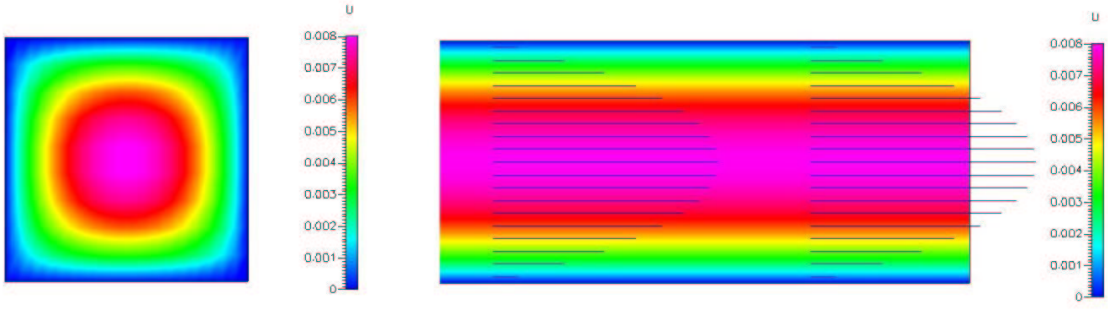

Figure 6.12: *3D CFD-ACE simulation of flow in the sample pretreatment system. To the left, a cross sectional view perpendicular to the flow direction, to the right, a view plane parallel to the flow direction. The unit for the color bar is m/s. In the image to the right a set of velocity vectors showing the magnitude of the flow at different positions in the channel is included. The total volumetric flow is 40μL/min. A typical parabolic flow profile is obtained with zero flow velocity at the channel walls. The maximum flow velocity is 8mm/s, with an average flow velocity of 4mm/s.*

To the left in figure 6.12 a cross sectional view perpendicular to the flow direction is shown. In the center of the channel the flow velocity is up to 8mm/s and then it decreases towards the channel walls where there is zero flow. The average velocity is approximately 4mm/s. To the right in figure 6.12 a view plane through the center of the channel parallel to the flow direction is shown. A set of velocity vectors showing the magnitude of the flow at different positions in the channel is included. It can be seen that the velocity profile describes the typical parabolic flow profile of laminar flow.

In the sample pretreatment the sample in form of whole cells are captured at the DEP electrodes at the bottom of the channel during the sample treatment, see figure 6.3. After the release they are to be transported to the PCR chamber. However, because of the parabolic flow profile, the cells, which also after the release are generally positioned near the bottom of the flow channel, will move slower than the average velocity of the liquid. This will cause a dilution of the cells as the velocity will depend strongly on

the exact position in the flow channel. But it also means that the amount of liquid needed to transport the cells into the PCR chamber is larger than the volume of the sample pretreatment part of the fluidic system. This is why the transportation of the cells into the PCR chamber is done using PCR mastermix solution, see figure 6.6. This way the the change in composition of the mastermix solution in the PCR chamber will be minimized.

6.3.2 Flow into the PCR chamber

When the sample enters the PCR chamber there is an abrupt change in the geometry, from a 400μm wide channel to a 5000μm wide chamber. Figure 6.13 shows a simulation of the flow profile in the channels leading to and from the camber as well as inside the chamber. A total volumetric flow of 40μL/min is used.

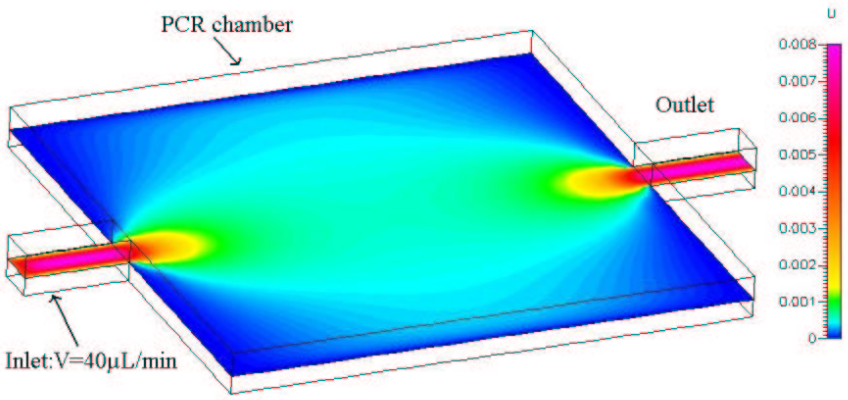

Figure 6.13: *3D CFD-ACE simulation of flow entering and exiting the PCR chamber. The flow velocity shown is for a view plane cut parallel to the substrate through the middle of the channel and PCR chamber. The total volumetric flow is 40μL/min. The flow velocity drops quickly when the flow enters the chamber, and there is virtually no flow in the corners of the PCR chamber*

The flow velocity shown in figure 6.13 is for a view plane cut parallel to the substrate, through the middle of the channel and chamber. The flow velocity, which is up to 8mm/s in the narrow channels, drops quickly when the flow enters the large chamber. The flow velocity in the middle part of the chamber is higher than in the outer parts near the edges of the chamber, and in the four corners there is virtually no flow.

As the sample will follow the shape of the flow profile in figure 6.13 it can be expected that the cells will only be transported to the central parts of the PCR chamber and not out into the corners.

6.4 Summary

In this chapter the design of a PCR chip with integrated DEP based sample pretreatment system has been presented. The device consisted of three components: a DEP based sample pretreatment system, a PCR chamber with integrated thin film heaters and temperature sensor to control the PCR thermocycling and a fluidic system that connects the two parts. The sample pretreatment system used the cell capture technique for sample treatment. Thermal and fluidic simulations were used to evaluate the expected performance of the device.

Chapter 7

Fabrication of PCR chip with integrated sample pretreatment

In this chapter the fabrication sequence for the PCR chip with integrated DEP based sample pretreatment system is presented. Two versions have been fabricated, version I and version II. In version I, the electrode material for the DEP structures can be different than the material used for the thin film heaters and temperature sensor that control the PCR thermocycling. In version II, the same electrode material is used for both the DEP and the heater structures. Finally the packaging method for the chip is presented.

7.1 Fabrication

Figure 7.1 shows the mask layout for version I of the integrated chip. Mask 1 is the metallization mask that defines the DEP structure for the sample pretreatment system. Two separate arrays of castellated electrode structures for cell capture are defined using this mask. Mask 2 is the metallization mask that defines the thin film heaters and temperature sensor that control the PCR thermocycling. Mask 3 defines the protection layer for the PCR electrodes. There is no protection layer at the DEP electrode structures, and the protection layer is also removed at the bond pads for the PCR electrodes. Finally, mask 4 defines the fluidic system that connects the DEP based sample pretreatment structures with the PCR chamber. Masks 1-3 are clear field masks, while mask 4 is a dark field mask.

The mask layout for version II is identical to the mask layout of version I shown in figure 7.1, except that the mask defining the DEP structures, mask 1, and the mask defining the PCR electrodes,mask 2, have been joined into a single mask. Thus in version II of the design, the DEP electrodes and the heater electrodes are made of the same material. This makes the fabrication procedure simpler.

In version I, where the material for the DEP electrodes can be different from the material for heater electrodes, nickel silicide have been used as DEP electrode material while

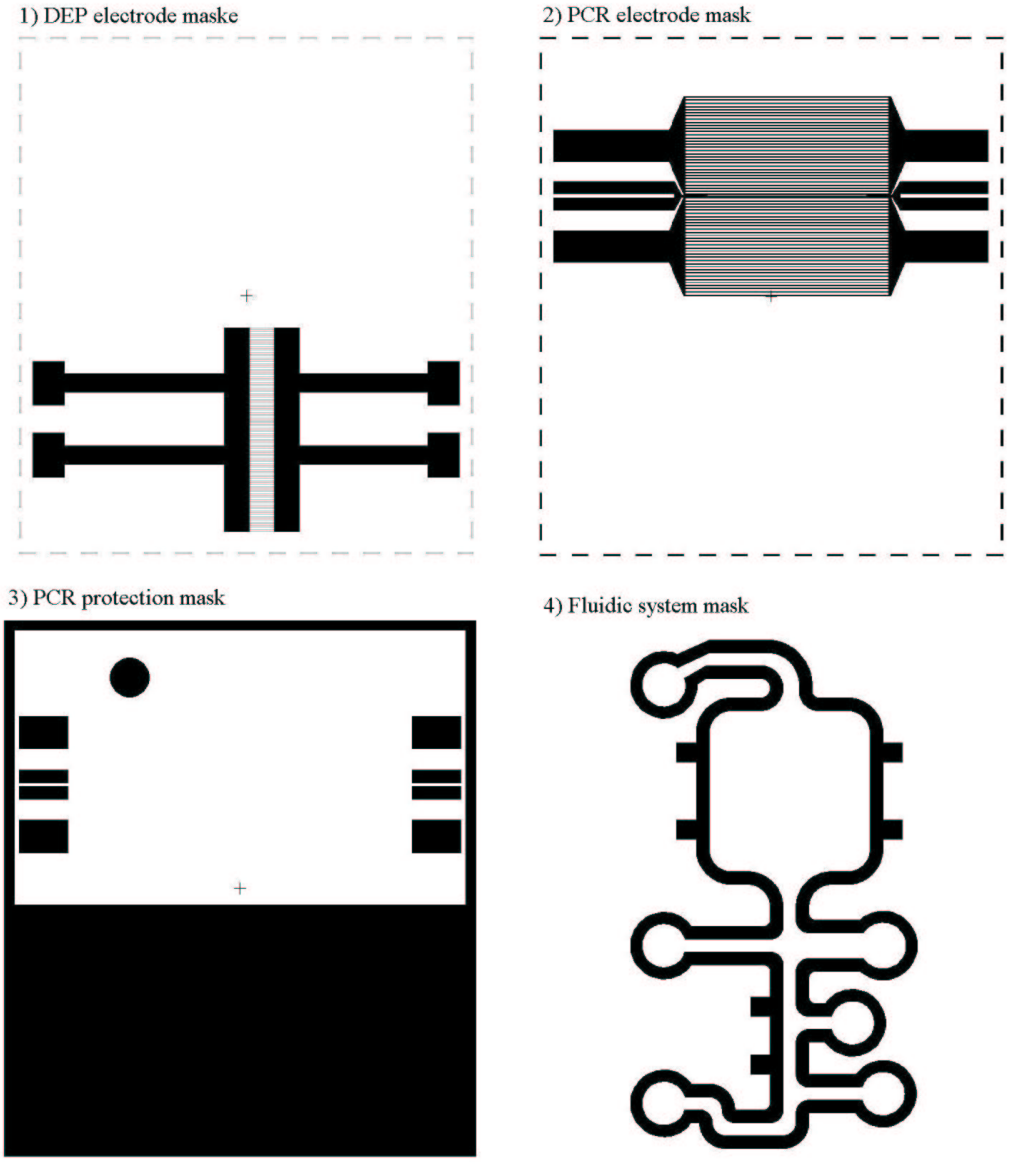

Figure 7.1: *Mask layout for version I of PCR chip with integrated DEP based sample pretreatment system. Mask 1 is for definition of DEP electrodes in the sample pretreatment system. Mask 2 defined the electrodes that control the PCR thermocycling. Mask 3 defines the protection layer for the PCR electrodes. Mask for id for definition of the fluidic system and the PCR chamber. Mask 1-3 are clear field masks, mask 4 is a dark field mask.*

platinum has been used for the PCR electrodes. The fabrication procedure, shown in figure 7.2 is basically a combination of the fabrication procedure for silicide electrodes on glass substrates, presented in section 5.5, with the fabrication procedure for the PCR chip, presented in chapter 3. Fused silica has been used as substrate material, but

borosilicate can also be used. Version II, which will be presented later, is fabricated on borosilicate substrates using nickel silicide for both the DEP and PCR electrodes. The detailed process sequence for both version I and version II can be found in appendix D.

4 inch 500μm thick fused silica wafers from Hoya corporation [103] are used as substrates. The wafers are cleaned in piranha (4:1 H_2SO_4:H_2O_2) and rinsed in water. A 100nm LPCVD polysilicon layer is deposited as shown in figure 7.2.1. This layer will be used to form the silicide for the DEP based sample pretreatment system. If borosilicate substrates are used, then the silicon has to be sputter deposited due to process compatibility issues.

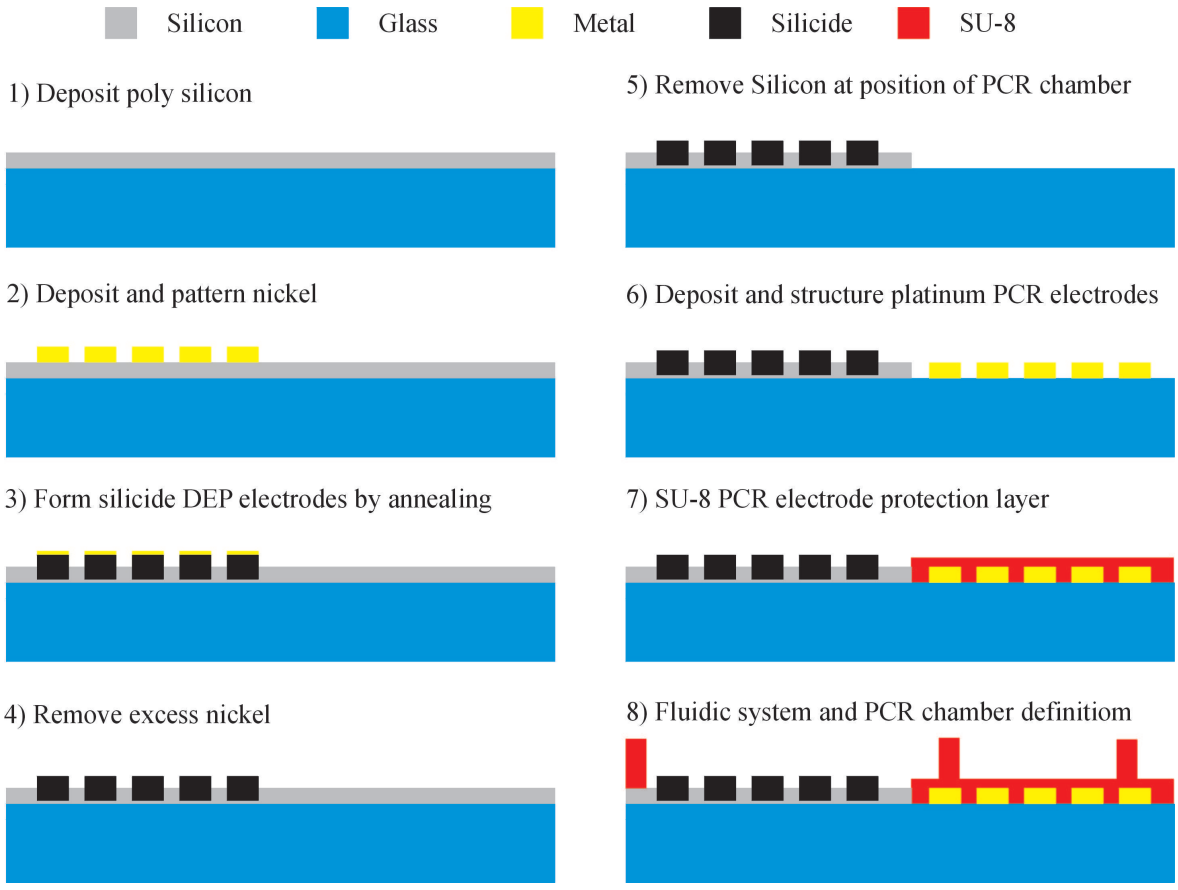

Figure 7.2: *Schematic of process sequence for version I of PCR chip with integrated DEP based sample pretreatment system. The chip is realized by 5 photolithographic steps, using the 4 masks shown in figure 7.1. Mask 3 is used twice.*

1.5μm AZ5214E photoresist is spun onto the wafer and structured with the DEP electrode mask, mask 1 in figure 7.1, using the image reversal process. 60nm nickel is deposited on the wafer using e-beam evaporation. A 30 second HF dip is applied just before the deposition of the metal to remove the natural oxide on the silicon. The nickel is structured using a lift off process in an ultrasonic assisted acetone bath, figure 7.2.2.

The silicide is formed using rapid thermal annealing (RTA) for 15 minutes at a temperature of 425°C in an argon atmosphere, figure 7.2.3.

Any excess nickel left after the formation of the silicide is removed in a piranha (4:1 H_2SO_4:H_2O_2), figure 7.2.4.

To the left in figure 7.3 an optical image of part of the two nickel silicide DEP electrode arrays is shown. There are no signs of cracking or flaking of the nickel silicide, as was previously experienced with titanium silicide on fused silica substrates.

Next the silicon is removed at the position of the PCR chamber. This is done by wet etching of the silicon using photoresist as mask. 1.5μm AZ5214E photoresist is spun onto the wafer and structured with the electrode protection mask, mask 3 in figure 7.1. The exposed silicon is removed using a polysilicon wet etch (20:1:20 HNO_3:HF:H_2O). The resist mask is removed after the etch in an ultrasonic assisted acetone bath, figure 7.2.5. The reason for the removal of the silicon is to make sure that the PCR electrodes are completely insulated from each other to prevent cross talk between the thermometer electrode and the heater electrodes. At elevated temperatures poly silicon will start to conduct.

The platinum thin film heaters and temperature sensor for the PCR thermocycling are structured using a lift-off process. To improve resist adhesion to the fused silica substrates, the wafers are treated with hexamethyldisilizane (HMDS) prior to the spinning of the resist. A 1.5μm thick AZ5214E resist is then spun onto the wafer and patterned using the image reversal lithography process and the PCR metallization mask, mask 2 in figure 7.1. The resist is hardbaked on a 120°C hotplate for 2 minutes, whereafter 150nm of platinum is deposited using e-beam evaporation. A 100Å titanium adhesion layer is used. The platinum is structured using lift-off in a ultra-sonic assisted acetone bath for 5 minutes, figure 7.2.6. If borosilicate substrates are used, then the resist adhesion needs to be improved by using a thin aluminum layer as described in section 3.1 on page 39.

Figure 7.3 to the right shows an optical image of part of the platinum heater structures and nickel silicide DEP structure. The image is taken with bottom illumination. The polysilicon used to form the silicide is removed at the position of the PCR chamber, but is still present at the position of the nickel silicide DEP structures.

A thin layer of SU-8 is used to protect the thin film PCR electrodes. To improve the adhesion of SU-8 the wafers are dehydrated by baking in a 250°C oven for more than 3 hours prior to the spinning of SU-8. Immediately after the wafer has cooled a 5μm SU-8 layer (XP2005, Microchem [85]) is spun onto the wafer with a rotation speed of 3000 rpm. The resist is soft baked for 3.5 minutes at 90°C and patterned by exposure through the PCR protection mask, mask 3 in figure 7.1, followed by a cross link bake. The cross link bake is done on a hotplate ramped from room temperature to 95°C in 5 minutes, staying at 95°C for 8 minutes, ramping to 105°C in 2 minutes and staying at this temperature for another 10 minutes. The wafers are left to cool on the hotplate for

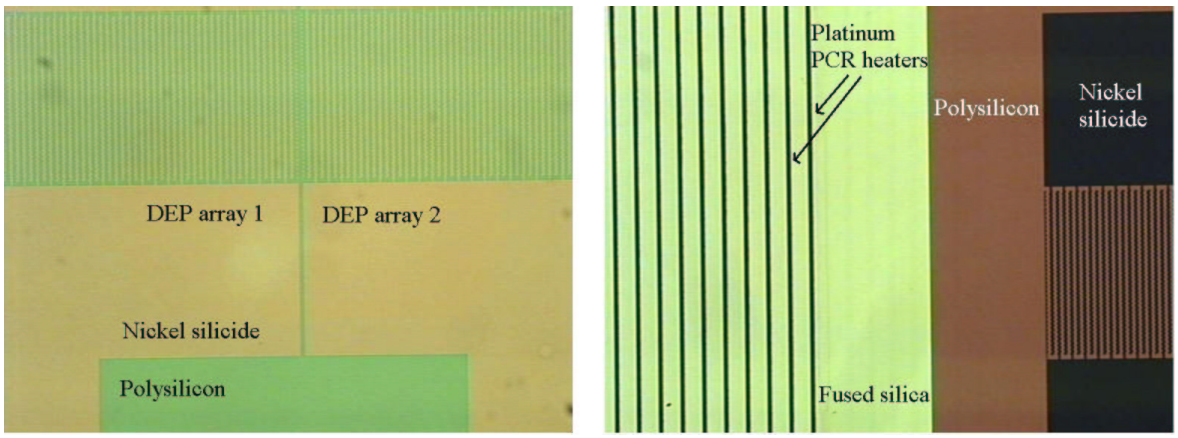

Figure 7.3: *Optical images of electrodes from integrated PCR chip version I. To the left part of the two nickel silicide DEP arrays for the sample pretreatment system is shown. To the right part of the platinum electrodes for the PCR thermocyling and part of the DEP electrodes are shown. The image to the right is taken with bottom illumination.*

the approximately 60 minutes it takes to reach room temperature. Figure 7.2.7 shows the cross linked part of the SU-8 protective layer. However, the layer is not developed yet.

The final step in the process is to define the SU-8 based PCR chamber and the fluidic system that connects it to the DEP based sample pretreatment system. This is done with a multi spin procedure to achieve a 400μm thick SU-8 layer. 200μm SU-8 (XP2075, Microchem [85]) is spun onto the wafer using a rotation speed of 1000 rpm and then soft baked on a hotplate for 45 minutes at 95°C using a temperature ramp of 10 minutes. The wafer is cooled on the hotplate until room temperature is reached. The spin and bake procedure is the repeated once more to realize a layer with a total thickness of 400μm. The PCR chamber walls and the channel systems are defined by exposure through the fluidic system mask, mask 4 in figure 7.1, followed by a cross link bake for 35 minutes at 95°C using a temperature ramp of 10 minutes to reach the bake temperature. Again the the wafer is cooled on the hotplate until room temperature is reached. Finally, the SU-8 is developed in PGMEA for approximately 30 minutes and the chip has been realized, see figure 7.2.8.

Figure 7.4 shows an optical image of a final PCR chip with integrated DEP sample pretreatment system, version I. At the bottom part of the chip the DEP based sample pretreatment system is located. The PCR chamber is located at the top of the chip and is connected to the sample pretreatment system via a fluidic system in SU-8. The fluidic system is only just visible, while the thin SU-8 layer that protects the PCR electrodes is not visible. The top part of the chip is transparent because the excess polysilicon, which was not used to form the nickel silicide electrodes in the DEP arrays, has been removed at the position of the PCR chamber in version I of the chips.

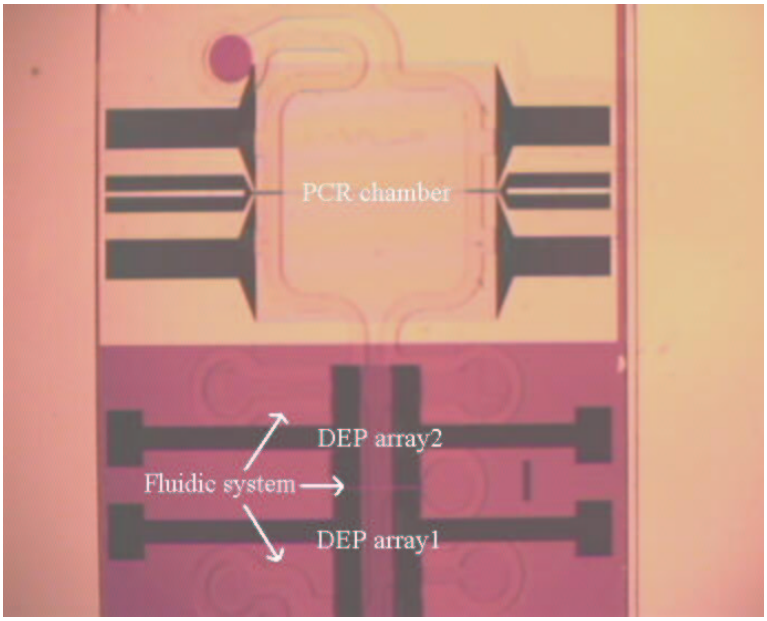

Figure 7.4: *Optical image of integrated PCR chip version I. At the bottom part of the chip the DEP based sample pretreatment system is located. The PCR chamber is located at the top of the chip and is connected to the sample pretreatment system via a fluidic system in SU-8.*

Fabrication of version II of the integrated chip is simpler than version I, as the DEP electrodes and the PCR electrodes are fabricated in the same mask step. Nickel silicide was used as the electrode material and and 1mm borosilicate was used as substrate. Fused silica can also be used as substrate. However, when borosilicate is used, the silicon where the silicide is formed, needs to be deposited by sputter deposition for process compatibility issues.

Both the DEP electrodes and the PCR electrodes are fabricated in one mask step during what is equivalent to step 3 and 4 in figure 7.2. Because of this, the step where silicon is removed at the position of the PCR chamber, see figure 7.2.5, has been omitted. Besides these changes the fabrication procedure of version II is identical to the fabrication procedure of version I presented above.

As mentioned earlier the reason for the removal of the silicon is to insulate the PCR electrodes from each other to prevent cross talk between the thermometer electrode and the heater electrodes. However, experiments with version II, showed that even when the silicon is not removed, cross talk is not a problem. Step 5 in figure 7.2 can thus also be omitted in version I, simplifying this process also.

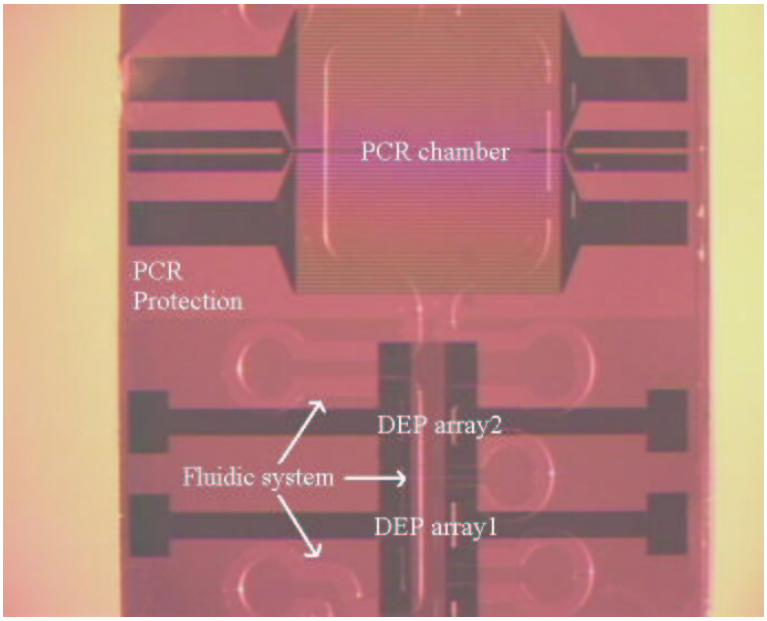

Figure 7.5: *Optical image of integrated PCR chip version II. In this version of the chip the polysilicon is not removed at the position of the PCR chamber. The slight color difference between the top part of the chip, where the PCR chamber is located, and the bottom part, where the sample pretreatment system is located, is due to the thin SU-8 layer that protects the PCR electrodes.*

Figure 7.5 shows an optical image of a final PCR chip with integrated DEP sample pretreatment system, version II. The DEP sample pretreatment system is at the bottom of the chip and is connected to the PCR chamber at the top of the chip via the SU-8 based fluidic system. The excess polysilicon is not removed at the position of the PCR chamber in version II of the integrated chips as was done in version I, see figure 7.4. The thin layer of SU-8 used to protect the PCR electrode can be observed as a slight color change between the bottom and top part of the chip.

Before use the chips are silanized with dichlorodimethylsilane, using the gas phase silanization procedure described in section 3.2 on page 42. The silanization enhances the PCR compatibility of the SU-8 surfaces in the PCR chamber.

7.2 Packaging

A schematic of the packaging method for the PCR chip with integrated sample pretreatment is shown in figure 7.6. The packaging method very similar to the chip carrier packaging presented for the PCR chip in section 3.4 and the DEP chip in section 5.4.3. The chip is mounted in a ceramic chip carrier placed in a metal holder. The chip carrier acts as a heatsink for the PCR thermocycling. Wire bonding is used for the

electrical interconnections to both the DEP electrodes and the PCR electrodes. Fluidic interconnections are drilled through the chip and chip carrier and a PDMS bonded lid is used to seal the fluidic system. There is optical access to the chip through the lid.

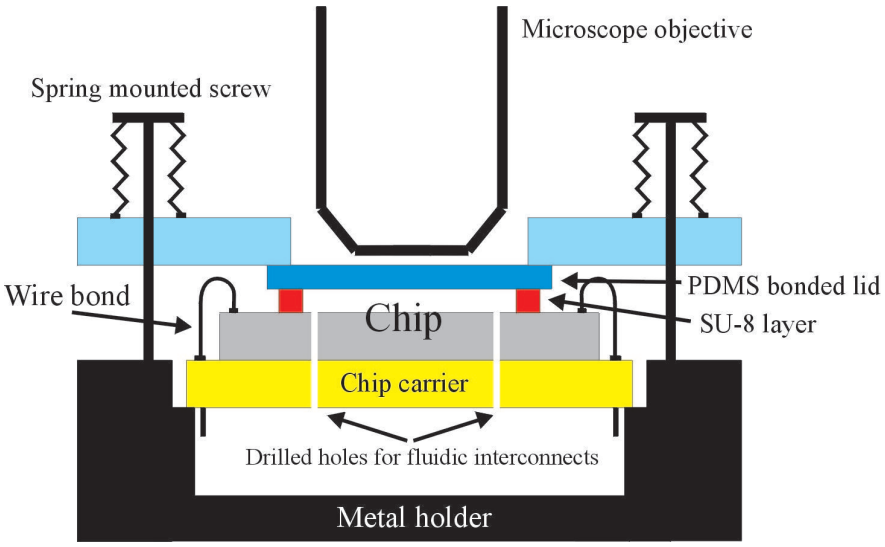

Figure 7.6: *Schematic of packaging of integrated PCR chip. The chip is placed in a ceramic chip carrier and electrical connections to the PCR electrodes and the DEP array is made using wirebonding. The chip carrier also acts as a heatsink for the PCR thermocycling. Fluidic interconnects are drilled through the chip and chip carrier. A PDMS pressure bonded lid is used to seal the device.*

7.3 Summary

The fabrication process for the PCR chip with integrated DEP based sample pretreatment system has been described in this chapter for version I and version II of the chip design. In version I of the design, the electrodes for the DEP based sample pretreatment system and the PCR electrodes are fabricated separately. In version II the DEP electrodes and the PCR electrodes are fabricated in single mask step simplifying the fabrication process. Version I was realized using nickel silicide DEP electrodes and platinum PCR electrodes. In version II both the DEP electrodes and the PCR electrodes were made of nickel silicide. A packaging method that seals the chip with a PDMS bonded lid while providing electrical connection and connection to a heatsink has also been presented.

Chapter 8

Characterization of PCR chip with integrated sample pretreatment

In this chapter initial characterization of the PCR chips with integrated sample treatment prior to PCR amplification will be described. The characterization will include both physical performance of the PCR chips, such as power consumption and cooling rates, as well as test of the sample pretreatment functionality. The physical performance will be compared to the predictions from thermal simulations of the design in chapter 6. Testing of the integrated PCR chip is still in its initial phases. Only a few results with respect to validation of the functionality of the integrated PCR chip will be presented here. More results and detailed information about the bio assays and the experimental setups can be found in [88, 83].

8.1 Setup

The setup for the integrated PCR chip combines the previous presented setup to control PCR thermocycling (see section 4.1) with electronics to control DEP and with a pump setup for fluidic handling. The PCR thermocycling and DEP electronics are Labview controlled. Details about the setup can be found in [88].

Figure 8.1 shows optical images of chip packaging (to the left) and parts of the setup (to the right). The integrated PCR chip is packaged using the chip carrier method described in section 7.2. The chip carrier package is then positioned in a microscope setup and connected with pump systems for fluidic handling (see figure 8.1) and the Labview based control systems for PCR thermocycling and DEP.

8.2 Physical characterization

In this section the physical performance of the integrated PCR chips will be characterized. This will include both power usage and cooling rates. Version I of the design uses a 500μm fused silica substrate, while version II uses a 1000μm borosilicate substrate. The emphasis in this chapter will be on version I of the integrated design. Most of the thermal performance characteristics presented for the PCR chip in section 2.3

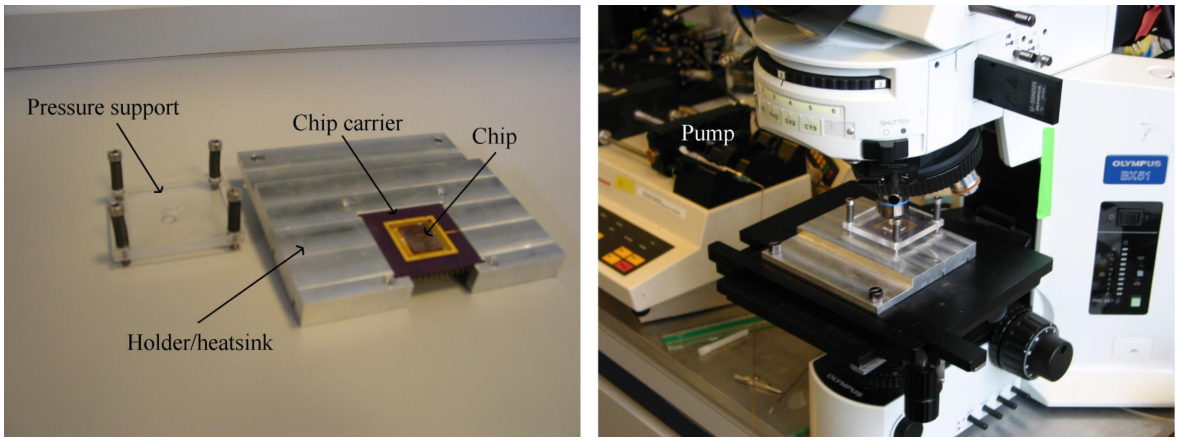

Figure 8.1: *To the left: Optical image of the chip carrier packaging method. The chip is mounted in a ceramic chip carrier that acts as heatsink during the PCR thermocycling and provides electrical connection to the chip. The chip and chip carrier is placed in a metal holder that provides support for the PDMS pressure bonded lid. To the right: The chip carrier package is placed in a microscope setup that provides optical access to the DEP based sample pretreatment system. Parts of the pump setup used for the fluidic handling can be seen in the background of the image.*

also apply for version II of the integrated design, as these chips are identical besides a difference in the size of the PCR chamber. The results will be compared to the simulations of the integrated PCR chip found in the design and simulation chapter 6. 500μm polymer lid were used for all the tested chips.

8.2.1 Calibration of thermometers

As with the previously presented PCR chip, the build in thermometer in the integrated PCR chip has to be calibrated before use. This is done in a temperature controlled oven, where the resistance of the thermometer is measured at different temperatures between room temperature and 100°C. Depending on the version of the design, the thermometer material can be either platinum (version I) or nickel silicide (version II). Figure 4.2 shows typically obtained calibration curves for both versions of the integrated PCR chip.

From figure 8.2 it is seen that the resistance of the build in thermometer varies linearly with temperature, regardless of the thermometer material. The behavior can be described by equation 4.2-1 on page 50, which gives a temperature coefficient of resistance (TCR) value α for the nickel silicide thermometer of $\alpha \sim 29 * 10^{-4}$. The TCR value for the platinum thermometer is again $\alpha \sim 30 * 10^{-4}$, similar to what was found for the previously presented PCR chips that also uses platinum thermometers. In the temperature region for PCR, nickel silicide thus functions similar (comparable TCR values) to platinum as material for resistive thermometers.

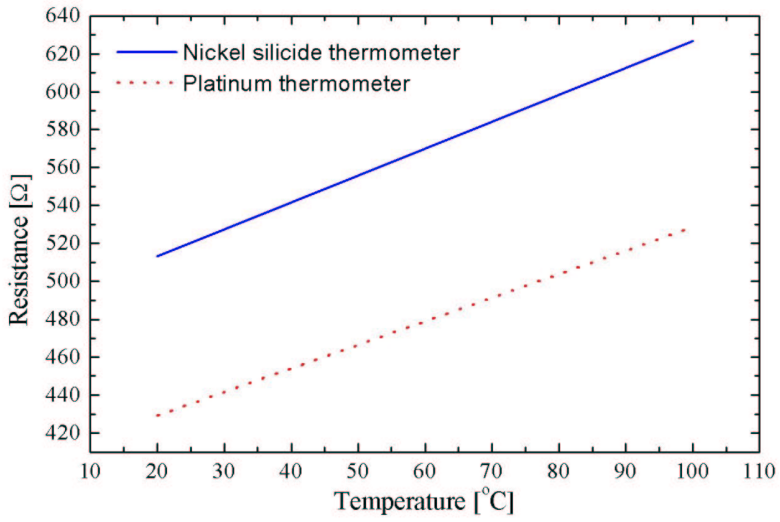

Figure 8.2: *Calibration curves of the resistive thermometers for version I and II of the integrated PCR chip. Version I uses a platinum based thermometer, while version II uses a nickel silicide thermometer. As the slopes of the two calibration curves are similar, the TCR values of nickel and platinum are comparable. In this temperature region nickel silicide resistive thermometers thus function similar to traditional platinum based thermometers.*

8.2.2 Power consumption

The power consumption of the integrated chip is dependent on the thickness and material of the substrate. But it is also dependent on the thermal contact between the chip and the heat-sink. To assure good thermal contact, heat conducting paste can be used between the chip and the heat-sink. However, when fluidic interconnects are drilled through chip and chip carrier, which is the case for normal operation of the device, the chips are mounted in the carrier using a cyanoacrylate based adhesive material. The thermal conductivity of this material is quite low ($\lambda \sim 0.1 W/\mathrm{m\ K}$) and depending on the thickness of the adhesive layer, lowering of the power consumption of the device can be expected.

In table 8.1 measured and simulated power consumption at 94°C, for chips with a 500μm fused silica substrate (Version I) and 1000μm borosilicate substrate (version II), are given. Like previously, the estimated heat-loss in the on-chip interconnects have been subtracted for the measured values. Heat conducting paste has been used to assure good thermal contact between chip and heat-sink, so the measured values can be compared to predicted power consumption from 3D CFD-ACE simulations.

Table 8.1: *Measured and simulated power consumption of the integrated PCR chip at 94°C*

Substrate	Chip version	Measured	3D CFD-ACE
500μm fused silica	Version I	$\sim 7.0W$	7.8W
1000μm borosilicate	Version II	~3.3W	3.4W

The measured and simulated power consumption for the chips realized on a 1000μm borosilicate substrate (version II) are in good agrement, with 3.3W and 3.4W, respectively. Because a smaller chamber is used, the power consumption of the integrated PCR chip design is lower, compared to the previously presented PCR chip, that was also realized on 1000μm borosilicate substrates. The difference in the power consumption correspond the the difference in the area spanned by the heaters in the two devices. As expected the measured power consumption for the integrated PCR chip realized on 500μm fused silica substrates is relatively high. A power consumption of 7.0W is measured, more than twice the value of the power consumption of devices realized on 1000μm borosilicate substrates. However, this is still lower than the 7.8W predicted by the CFD-ACE simulation. This is presumably due to less than perfect contact between chip and heat-sink, even when heat conducting paste is used. As will be discussed next, the power consumption is very dependant on the contact between chip and heat-sink, especially for chips realized on 500μm fused silica substrates.

The effect of having a non perfect contact between chip and heat-sink, e.g. when an adhesive is used to mount the chip, can be estimated by a simple addition to the previously presented 1D model (see figure 2.2 on page 20). We know from the model that almost all heat is lost by conduction through the substrate, so the heat-loss through the lid can be neglected. If a layer of another material with thickness t_2 and thermal conductivity λ_2 is placed between the chip and the heat-sink, then the total power consumption pr unit area can be estimated by equation 8.2-1.

$$P = \dot{Q} = A \left[\frac{t_2}{\lambda_2} + \frac{t_1}{\lambda_1} \right]^{-1} \Delta T \tag{8.2-1}$$

A is the area spanned by the heaters, t_1 is the thickness and λ_1 is the thermal conductivity of the substrate. ΔT is the temperature difference between chip and heat-sink.

The additional layer between chip and heat-sink increases the thermal resistance, thus decreasing the power consumption. Because of the low thermal conductivity of the cyanoacrylate based adhesive used to mount the chips, even a thin layer can have a great effect on the power consumption. A 50μm adhesive layer ($t_2 = 50\mu$m, $\lambda_2 = 0.1W/m\ K$) will lower the power consumption of the devices realized on 500μm fused silica substrates ($t_1 = 500\mu$m, $\lambda_1 = 1.4W/m\ K$) by ~60%. Power consumption of devices realized on 1000μm borosilicate substrates ($t_1 = 1000\mu$m, $\lambda_1 = 1.1W/m\ K$) will be ~35% lower with a 50μm adhesive layer .

It is hard to estimate the thickness of the adhesive layer used when mounting the chips and the thickness will vary from chip to chip. However, measured power consumptions 50-70% lower than when heat conduction paste is used, has been observed for the chips realized on 500μm fused silica substrates.

8.2.3 Cooling rates

Like the power consumption the cooling rate of the chips will depend on both the substrate used and the contact to the heat-sink. In figure 8.3 a measurement of the temperature drop of a integrated PCR chip from 94°C when the power to the heaters are turned off is shown. The chip is realized on a 500μm fused silica substrate. The temperature is measured by the build in resistive thermometer. Included in the figure is 1D SPICE simulation of the temperature drop. Heat conducing paste has been used between chip and heat-sink so the measured values can be compared to simulations.

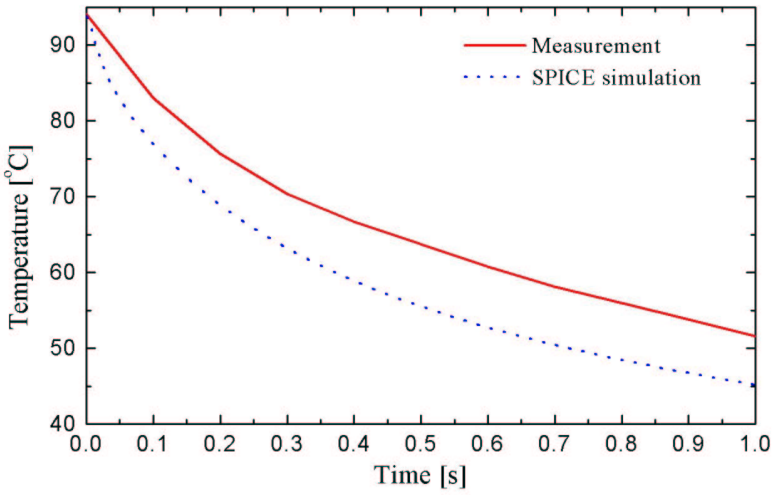

Figure 8.3: *Measurement of the temperature drop from 94°C for an integrated PCR chip realized on a 500μm fused silica substrate (100ms sampling rate). Included in the figure is a SPICE simulation of the temperature drop. The initial measured temperature drop is slower than predicted by the SPICE simulation, presumable due to effects from the packaging, including the contact between chip and heat-sink.*

The initial measured temperature drop of the PCR chip in figure 8.3 is slower than the SPICE simulations. The measured cooling rate between 90°C and 80°C is $\sim$ 100°C/s, where the SPICE model predicts a cooling rate of more than 150°C/s. As previously mentioned, the influence of the packaging, which is omitted in the simulation, will cause a slightly lower initial cooling rate. However, some of the effect may also be due

to non ideal contact between the chip and heat-sink, even when heat conducting paste is used. The measured average cooling rate between 90°C and 60°C is ∼ 60°C/s, with the SPICE model predicting a cooling rate of ∼ 85°C/s. However, most of the difference is caused by the initial lower cooling rate in the measurement compared to the simulation. Below ∼ 70°C the measured cooling rate correspond well to the simulated.

The cooling rate for the integrated PCR chip on 1000μm borosilicate substrates is identical to the cooling rates found for the PCR chip previously presented in section 2.5.4.

The cooling rates are also very dependent on the contact between chip and heat-sink. In figure 8.4 a measurement of the temperature drop of a integrated PCR chip mounted using the cyanoacrylate based adhesive is shown. The chip was realized on a 500μm fused silica substrate. The measured power consumption of this particular chip at 94°C was ∼ 2.6W, which is ∼60% lower than when heat conducting paste is used. According to the previous section, this correspond to a ∼ 50μm thick adhesive layer. Included in the figure is a 1D SPICE simulation of the temperature drop. The SPICE model is based on the previously presented model in chapter 2 (see figure 2.3), but with an 50μm cyanoacrylate layer between chip and heat-sink.

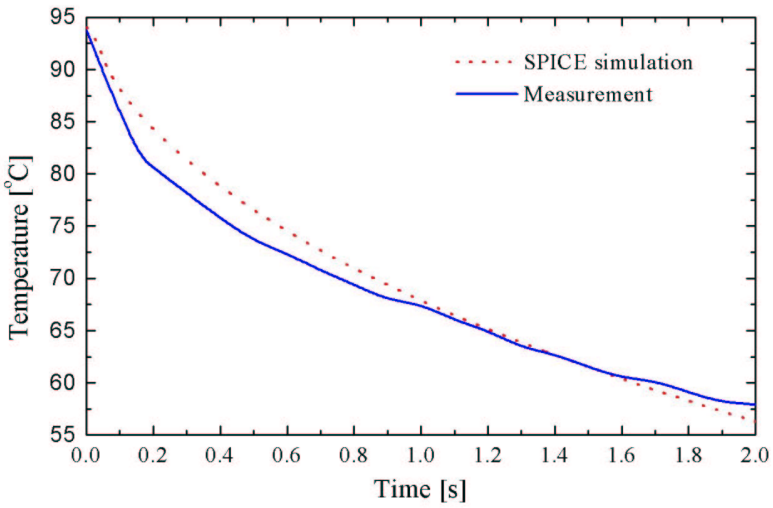

Figure 8.4: *Graph of measured and simulated cooling for a chip mounted with cyanoacrylate based adhesive. The chip is realized on a 500μm fused silica substrate and according to power consumption measurements the adhesive layer has a thickness of ∼ 50μm. The measured temperature drop (100ms sampling rate) is slightly faster than predicted by SPICE, but less than half as fast as when heat conducting paste is used during mounting of the chips.*

The initial measured temperature drop of the PCR chip in figure 8.3 is slightly faster than the SPICE simulation, but still much slower than when heat conducting paste is used (see figure 8.3). The measured cooling rate between 90°C and 80°C is ~ 50°C/s or about half the cooling rate measured when heat conducting paste is used. Both the measured and simulated average cooling rate between 90°C and 60°C is ~ 20°C/s, or less than a third of the cooling rate measured when heat conducting paste is used.

Even a $\sim 50\mu$m thick adhesive layer decreases the achievable cooling rates considerably when 500μm fused silica substrates are used. The effect of the adhesive layer on the cooling rates will be smaller for the chips realized on 1000μm borosilicate substrates. However, it is clear that the cyanoacrylate based adhesive used, was a bad choice. The chips should be mounted with an adhesive with larger thermal conductivity to avoid the large decrease in performance.

8.3 Test of fluidic system

The functionality of the fluidic system were tested with the following experiment: Yeast cells were captured and subsequently released from the sample pretreatment system and then transported with flow to the PCR chamber. Figure 8.5 shows optical images of the cell sample as it enters and exits the PCR chamber. The total volumetric flow is $\sim 30\mu$L/min.

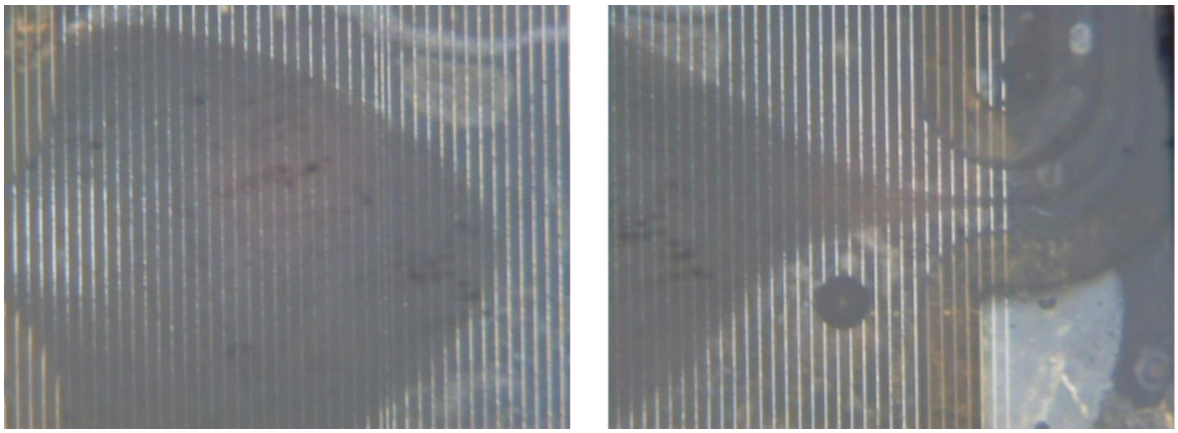

Figure 8.5: *Optical images of yeast cell sample entering (to the left) and exiting (to the right) the PCR chamber after being released from the sample pretreatment system. The total volumetric flow is $\sim 30\mu$L/min. the cell sample is only transported to the central parts of the PCR chamber and not out to the corner regions. However, there is more than ample amount of cells transported into the PCR chamber for PCR amplification.*

In the image to the left in figure 8.5 the cell sample (the dark "cloud") has entered the PCR chamber from the sample pretreatment system. The middle of the chamber

can be seen as the position where the thermometer electrode is embedded between the PCR heater electrodes. It can be seen that the sample has progressed furthest in the central part of the PCR chamber and that it only spreads slowly towards the edges of the chamber. This corresponds well with the simulated flow profile found in section 6.3 (see figure 6.13 on page 95). In the image to the right the cell sample has started exiting the PCR chamber. The sample is "squeezed" towards the central part of the chamber before exiting, in agrement with the simulation in section 6.3.

As expected the cell sample is only transported to the central parts of the PCR chamber and not out to the corner regions. However, there is more than ample amount of cells transported into the PCR chamber, and during the PCR thermocycling, DNA will diffuse to the outer regions of the PCR chamber.

Other experiments and detailed discussion about sample transport and fluidic handling in the integrated PCR chip can be found in [88]

8.4 Test of sample pretreatment system

To test the ability for sample pretreatment in the integrated chip, a mixture of yeast cells with a known amount of heparin was used. Heparin is a PCR inhibitor that, when present in sufficient amount, prevents PCR amplification [113]. Using the capture and wash sample pre-treatment technique (see figure 6.3), the yeast cells were captured at the electrode arrays while the heparin was washed out of the system. Both treated sample as well as non-treated sample was then subjected to PCR amplification. The samples were analyzed using an Agilent bioanalyzer 2100 with a DNA 500 chip kit. In figure 8.6 two superimposed electropherograms of the analysis is shown.

The PCR amplification of both the treated and non-treated sample was performed in a conventional PCR thermocycler as testing of the integrated PCR chip is still in its initial stages, and to make sure that potential silanization coating problems with the PCR chip would not influence the result. The amplification was of a 199 base pair fragment of yeast ribosomal S3 gene. As seen in figure 8.6 it was only in the treated sample that there was successfully amplified. The peak in the electropherogram of the treated sample at 70.5 seconds correspond to a $\sim$199 base pair fragment.

The sample pretreatment system is thus able to perform necessary treatment of sample prior to the PCR amplification. Other experiments and detailed discussion about sample pretreatment can be found in [88, 83].

8.5 Outlook

The testing of the integrated PCR chip is still in its initial stages and only simple sample pretreatment functionality has been performed. The constraints imposed by the DEP sample pretreatment system on the maximum conductivity of samples, to

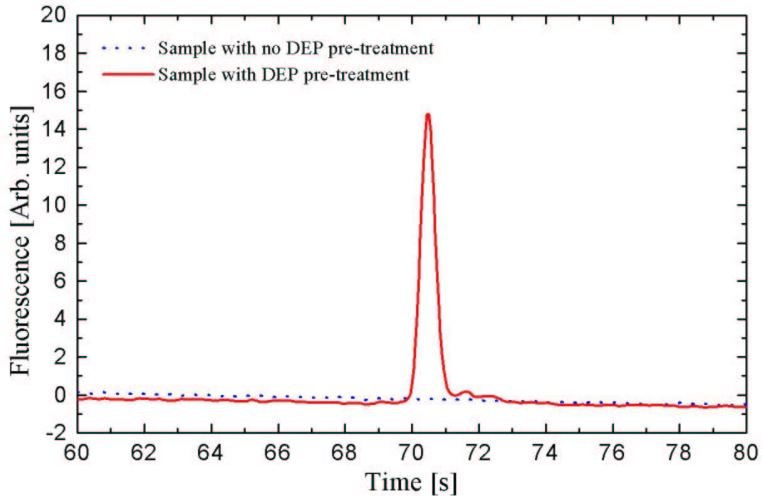

Figure 8.6: *Two superimposed electropherograms (Agilent bioanalyser 2100) of the analysis of PCR amplification of a 199 base pair fragment of yeast ribosomal S3 gene from sample with and without DEP sample pretreatment. Only the treated sample was successfully amplified (the peak at ∼70.5 seconds).*

some degree limits the type of samples that can be used in the system. The chip may not yet be capable of handling "real life" samples, but it represents one of the few examples of sample pretreatment performed on chip, which is one of the main challenges that remain in the development of true μTAS. As a further step towards true μTAS devices, the integrated PCR chip can potentially be expanded with other functionality.

A logical extension of the functionality of the integrated chip is a capillary electrophoresis (CE) system. SU-8 based CE chips fabricated on glass substrates have been presented in literature [114, 115], and can be implemented by a simple extension of the fluidic system at the PCR outlet. This can be done without any changes to the fabrication process. However, an addition of a CE system will of cause complicate the fluidic handling on the chip.

As mentioned in the introduction, integration of planar waveguides for optical detection could be used in both the sample pretreatment system and for real time monitoring of PCR. They could potentially also be used for detection in a CE system. In the next chapter the fabrication of SU-8 based planar waveguides will be presented. The waveguides can be integrated with the presented PCR chip without adding to the complexity of the fabrication process.

This ability to integrate multiple functionality without adding to the fabrication complexity is important. Increased fabrication complexity when integrating two devices will in most cases add limitations to the integrated functionality.

8.6 Summary

In this chapter characterization of the PCR chip with integrated DEP based sample pretreatment has been presented. Physical characterization showed good agrement between measurement and simulation when heat conducting paste was used for mounting the chips in the chip carrier. But it was also found that the thermal properties of the chip was very dependent on the contact between chip and heatsink, especially when a 500μm fused silica substrate is used. Initial tests of the sample pretreatment system showed that the PCR inhibitor heparin cold be removed from samples thus enabling successful amplification. The SU-8 based PCR chip can potentially also be integrated with other functionality such as CE for post PCR analysis and SU-8 waveguides for optical detection, without adding to the fabrication complexity.

Chapter 9

SU-8 based Polymer waveguides

In this chapter design and fabrication of planar polymer waveguides for use in μTAS devices is presented. The waveguides, the fluidic system and fiber-to-waveguide couplers are defined using a single mask step, thus ensuring self-alignment between the optics and the fluidics. By choosing SU-8 as the waveguide material a fabrication procedure which is compatible with the presented PCR chip with integrated DEP based sample pretreatment is obtained. This can be used in future integration of optical detection schemes for the presented PCR chip. However, in this thesis the waveguides have only been integrated with cell handling devices. The development of the SU-8 based waveguides was done in collaboration with Ph.D. student Klaus Bo Mogensen from the μTAS project at MIC, and application of the waveguides in micro chemical analysis systems can be found in [116, 117].

9.1 Design of SU-8 based waveguides

As mentioned previously (see section 1.3) planar optical waveguides can be used in a variety of different μTAS devices that rely on optical detection schemes. Of interest with respect to the topic in this thesis is real-time monitoring of PCR product, flow cytometry devices for cell handling and detection in CE chips for post PCR analysis. A design which integrates planar SU-8 waveguides with fluidic systems and that is compatible with the presented PCR chip is shown in figure 9.1.

Waveguidance by means of total internal reflection is obtained by having a waveguide core layer surrounded by buffer and cladding layers with lower refractive index. The SU-8 layer defining the waveguide cores and fluidic system is fabricated on a suitable substrate that acts as the buffer layer for the waveguide by having a refractive index lower than SU-8. SU-8 has a refractive index n$\sim$ 1.59 at 635nm (prism coupler, model 2010, Metricon [118]). The substrate can be glass (n$\sim$1.46), but in principle any substrate with n$<$ 1.59 compatible with SU-8 fabrication can be used. The fluidic system is sealed by a lid, that also acts as top cladding layer and therefore also needs to have a refractive index n$<$1.59. The PDMS lid used for the presented PCR chips have a refractive index of n$\sim$1.4 and can thus be used, but again any material with n$<$ 1.59

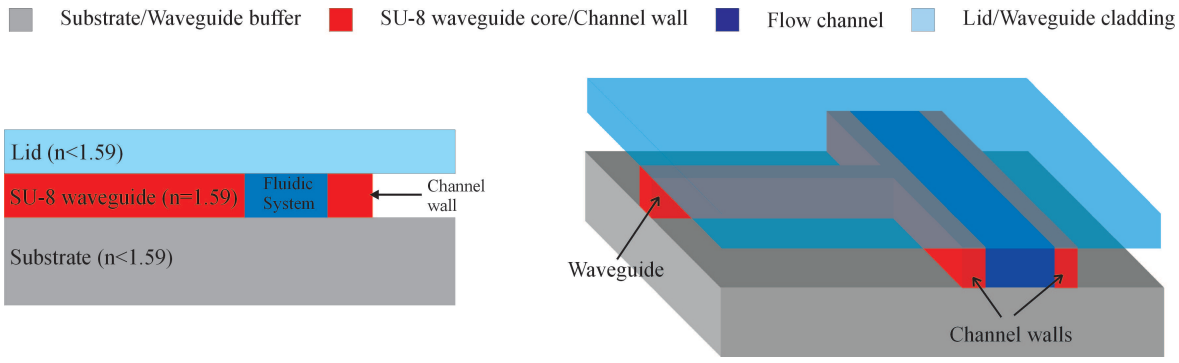

Figure 9.1: *Sideview (to the left) and general view (to the right) of SU-8 planar waveguides integrated with a fluidic system. Waveguidance by means of total internal reflection is obtained by having the SU-8 waveguide core layer surrounded by buffer layer (the substrate) and cladding layers with lower refractive index. The lid acts as top cladding layer, while air act as cladding on the side of the SU-8 waveguides.*

that can seal a fluidic system can be used. Air (n=1) act as cladding on the side of the waveguides.

In this thesis the waveguides are used in flow cytometry devices for velocity measurements of fluorescent cells/beads. The principle of the devices is that excitation light is guided to a fluidic system through two or more waveguides. Each time a fluorescent particle passes in front of one of the waveguides there will be a peak in the fluorescent signal. The time between the peaks in the fluorescent signal is then a measure of the velocity of the particle. The general SU-8 waveguide design can however be applied to many different application and examples of use in micro chemical analysis systems can be found in [116, 117].

In figure 9.2 two basic mask layouts for the flow cytometry structures are shown. Waveguides, a fluidic system and fiber-to-waveguide couplers are all defined using a single mask step, thus ensuring self-alignment between the optics and the fluidics. In the design to the left in figure 9.2 light is guided to the fluidic system through a 30μm wide waveguide with a 1x2 splitter. The waveguides are spaced by 200μm after the split. In the design to the right in the figure light is guided to the fluidic system through a 30μm wide waveguide with a 1x4 splitter. Either through a symmetrical 1x4 splitter where the spacing between the waveguides after the split is 150μm (to the left), or through a asymmetrical 1x4 splitter where the spacing after the split is 100μm,150μm and 200μm, respectively. The fluidic channel is 100μm wide, while the fiber-to-waveguide couplers consists of tapered grooves which are aligned to the planar waveguide structure. The groove structures have been designed to work with an optical fiber with an outer diameter of $\sim$70μm (FVP050055065, Polymicro Technologies [119]).

To avoid unguided light reaching the detection zone in the fluidic system the waveguides are bend by 20°. This introduces bend loos in the waveguides. However, by

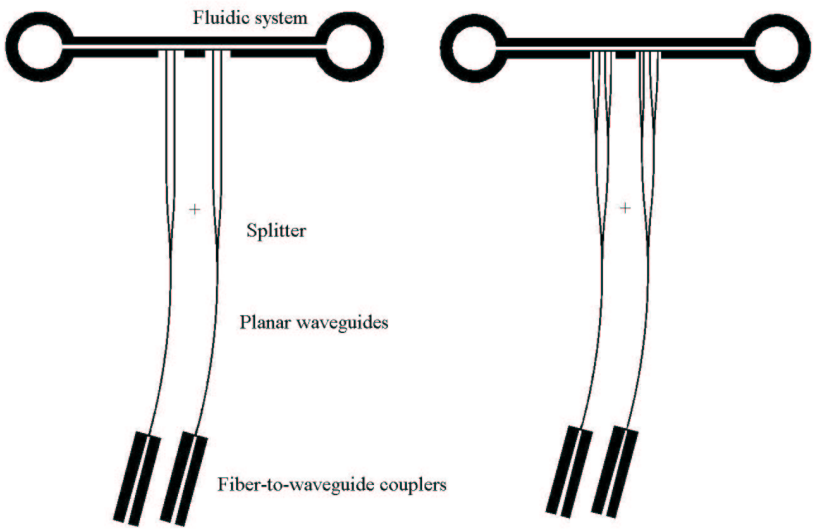

Figure 9.2: *Mask layout for flow cytometry structures. The fluidic system, the planar waveguides with splitters and fiber-to-waveguide couplers are defined in a single mask layer. In the design to the left the waveguides are split using a 1x2 splitter. In the design to the right the waveguides a split using ether a symmetrical or a asymmetrical 1x4 splitter.*

choosing a large ratio of 500 between the bend radius and the width of the waveguide the bend loss is negligible [120].

9.2 Fabrication and Packaging

The devices are fabricated on silicon substrates, see figure 9.3.1, but Borosilicate (n∼1.47-1.48, [84]) and fused silica (n∼1.46) can also be used as substrates. The detailed process sequence can be found in appendix E

A 2.5μm silicon dioxide layer is grown by annealing at 1100°C in water vapor for 16 hours (n=1.46 at 633nm), see figure 9.3.2. This layer will act as the waveguide buffer layer.

The final step in the process is to define the SU-8 waveguides and fluidic system. To improve the adhesion of SU-8 the wafers are dehydrated by baking in a 250°C oven for more than 3 hours prior to the spinning of SU-8. Immediately after the wafer has cooled a ∼90μm SU-8 layer (XP2075, MicroChem [85]) is spun onto the wafer using a rotation speed of 1800 rpm and then soft baked on a hotplate for 25 minutes at 95°C using a temperature ramp of 10 minutes to reach the bake temperature. The wafer is cooled on the hotplate until room temperature is reached. The structures are defined

by uv exposure ($\sim$ 900mJ/cm^2 at 365nm) through the waveguide mask, see figure 9.2, followed by a cross link bake for 25 minutes at 95°C using a temperature ramp of 10 minutes to reach the bake temperature. The wafers are cooled on the hotplate until room temperature is reached. Finally, the SU-8 is developed in PGMEA for approximately 10 minutes and the chip has been realized, see figure 9.3.3.

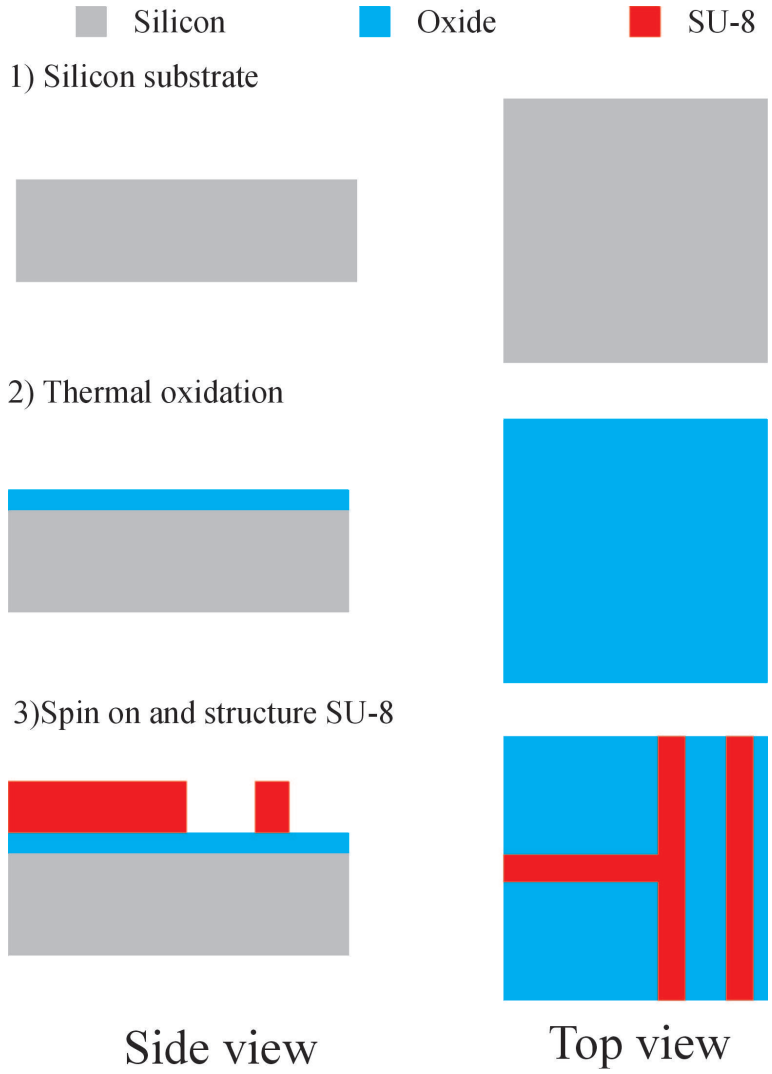

Figure 9.3: *Schematic of process sequence for polymer waveguide devices. The devices are realized using a single mask step that defines both the waveguide and the fluidic system.*

Figure 9.4 shows an optical image of one of the asymmetrical 1x4 splitted waveguides where the spacing after the split is 100μm,150μm and 200μm, respectively.

A schematic of the waveguide device packaging method is shown in figure 9.5. The packaging method is very similar to the chip carrier packaging presented for the DEP

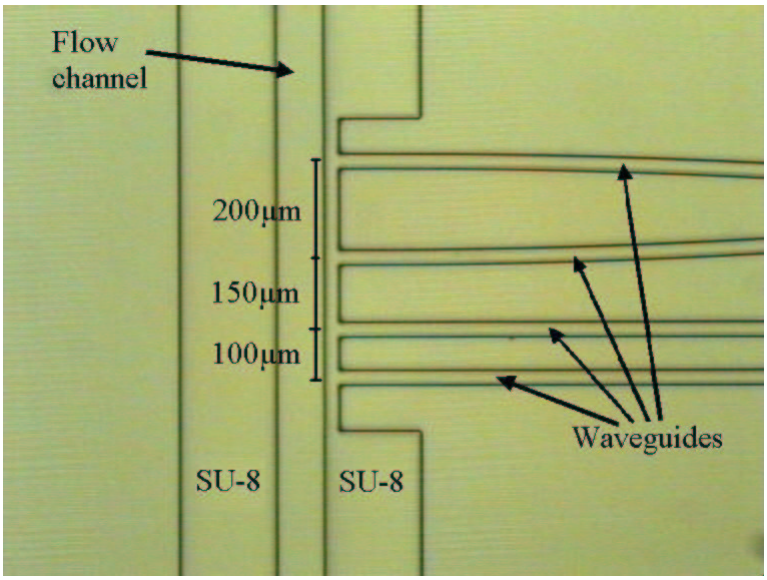

Figure 9.4: *Optical image of a flow cytometry device with a 1x4 asymmetrically split waveguide. The spacings between the four waveguides after the split are 100µm,150µm and 200µm, respectively.*

devices in section 5.4.3. A PDMS bonded lid is used to seal the fluidic system, and holes for fluidic interconnects are drilled through the chip and chip carrier. The advantage of this packaging method is that optical access through the lid is possible using microscope objectives.

An external fiber is coupled to the waveguides using the on chip fiber-to-waveguide coupler structures. Vertical alignment of the fiber is provided by extension of the lid over the coupler regions. The external optical fiber is simply inserted into the fiber-to-waveguide coupler as shown in figure 9.6. To make this possible the height of the SU-8 layer needs to be larger than the diameter of the optical fiber used.

The SU-8 based polymer waveguides are not only interesting because they offer potential integration with the cell handling and PCR devices presented previously in this thesis. The fabrication and packaging of the SU-8 based polymer waveguide devices is very simple and can be done in a single day. Typical integrated glass waveguides uses 2-4 photolithographic masks steps and a relatively complicated fabrication procedure taking weeks to complete [79, 80]. Use of polymer based waveguides can thus significantly reduce the total system cost.

9.3 Characterization of waveguides

The propagation loss of the SU-8 waveguides was calculated by measuring the transmission spectrum from 190nm-910nm (Spectro 320, Instrument systems [121]) on waveg-

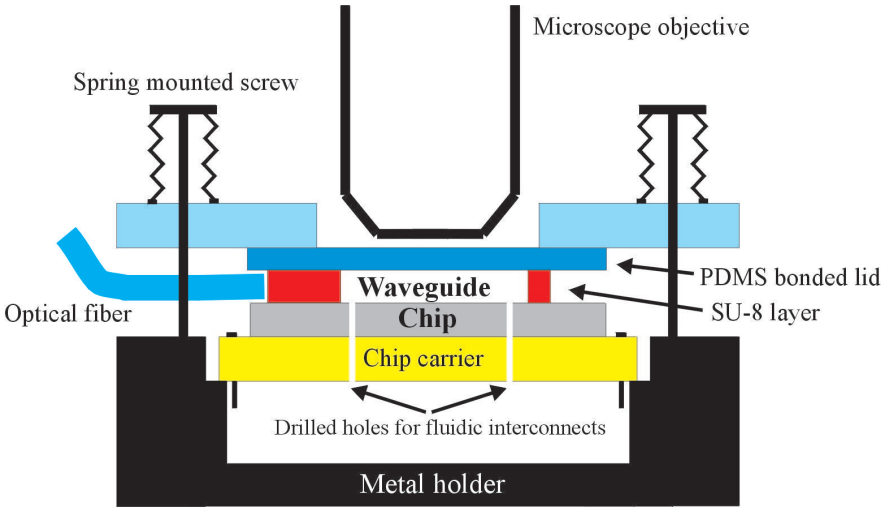

Figure 9.5: *Schematic of the waveguide device packaging. The waveguide chip is packaged using a ceramic chip carrier. Holes are drilled through chip and carrier for the fluidics connection. A PDMS bonded lid is used to seal the fluidic system. An external optical fiber is connected to the planar waveguides using the fiber-to-waveguide couplers on the chip. Vertical alignment of the fiber is provided by extension of the lid over the coupler regions. The fluidic system can be observed through the lid using a microscope objective.*

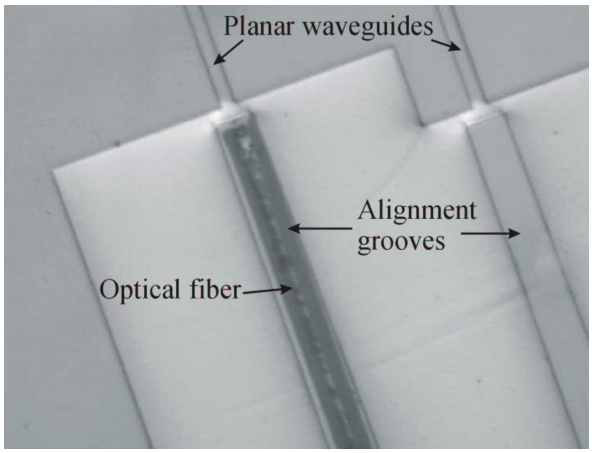

Figure 9.6: *Optical image of two fiber-to-waveguide coupler structure. In the coupler structure to the left an optical fiber has been inserted, while no fiber is inserted in the coupler structure to the right.*

uides of different length. The calculated propagation loss is shown in figure 9.7. Above ∼550nm the loss is less than 3dB/cm but it increases rapidly below 550nm. Both scattering and absorption contribute to the propagation loss in the waveguide. The rapid increase in the loss below 550nm is belived to be due to absorption in the SU-8

material. At 633nm the loss is 1.4dB/cm and at 850nm it is 0.8dB/cm which is the lowest reported for SU-8. In literature Lee *et al.*[81] have reported a propagation loss in SU-8 waveguides of 4 dB/cm at 633nm, while Curtis *et al.* [122] reported a loss of 6.2dB/cm at 850nm. The difference in the reported propagation losses can be due to the fact that the propagation loss in SU-8 is very sensitive to thermal degradation or "yellowing" [117]. Different process and post process treatments effects the performance of the waveguides.

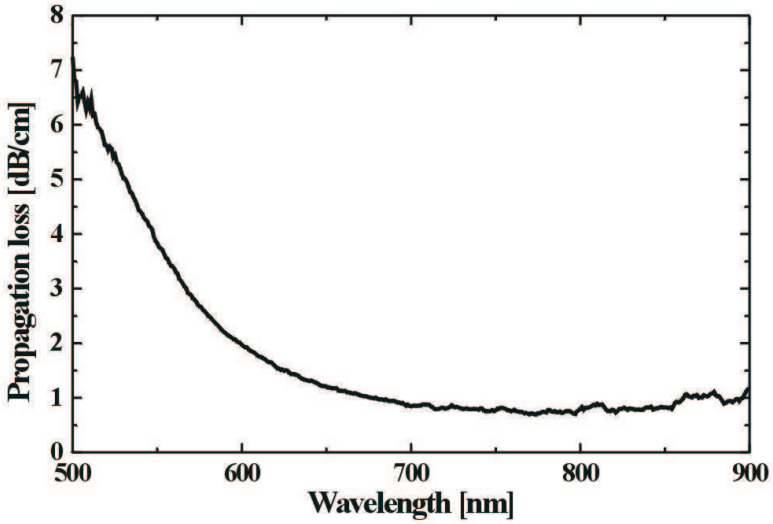

Figure 9.7: *Spectrally resolved propagation loss for planar SU-8 waveguides. The loss is caused by both scattering and absorption in the waveguides. Above ∼550nm the loss is less than 3dB/cm. Below 550nm the loss starts to increase rapidly.*

9.4 Flow cytometry measurements

A 488nm Ar ion laser has been used for fluorescent excitation in the flow cytometry measurements. As seen in figure 9.7 the propagation loss in the SU-8 waveguides is quite large below 500nm. However, due to the short length of the waveguides and the efficient coupling of light from external fiber to waveguide, ample light for fluorescent excitation is guided to the fluidic system. This is shown in figure 9.8 where light is guided to a fluorescein filled channel through a waveguide with a 1x2 splitter. There is a strong fluorescent signal in front of the two waveguides, where excitation light is coupled into the channel.

In a flow cytometry setup 6μm beads (Fluoresbrite YG, Polyscience) were pumped through the device with excitation light guided to the channel through a 1x2 splitter.

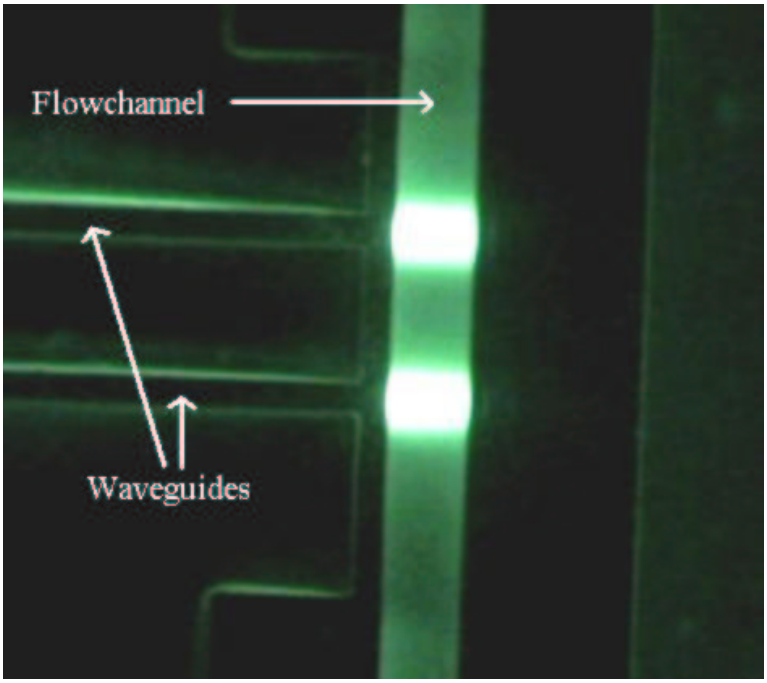

Figure 9.8: *Optical image of excitation light guided to a fluorescein filled channel through a 1x2 splitter. There is a strong fluorescent signal in front of the two waveguides, where excitation light is coupled into the channel.*

The fluorescence signal was measured using a photo multiplier tube (PMT). The signal from two beads flowing through the channel is shown in figure 9.9. A bead passing in front of the two waveguides results in two clear peaks (signal/noise ratio ∼10) in the fluorescence signal. The two waveguides are spaced 200 μm apart, thus the ∼20ms between a pair of peaks correspond to the two beads passing the waveguides with a velocity of $\sim 10mm/s$.

Although the velocity of the particles/cells can be found in experiments where light is guided to the flowchannel with a 1x2 splitted waveguide the direction of the motion can not be determined from the signal. In systems where the motion of the cell is caused by fluid flow the direction of the flow is usually known. However, if the cell is moved by TWD as in chapter 5, the direction of motion is unknown as it will depend on the properties of the cell. The asymmetrical 1x4 splitted waveguide device, shown to the right in figure 9.2, can be used to determine both velocity and direction of the cells. The spacing of the waveguides after the split is 100μm,150μm and 200μm, respectively. A particle passing the waveguides in one direction will result in four peaks in the fluorescence signal with a time spacing of x,1.5x and 2x. A particle passing in the other direction will result in peaks with a time spacing of 2x,1.5x and x, respectively.

Figure 9.10 shows the fluorescence signal from one bead passing in front of a 1x4 asymmetrically split waveguide. The four peaks have a spacing of approximately 2x, 1.5x

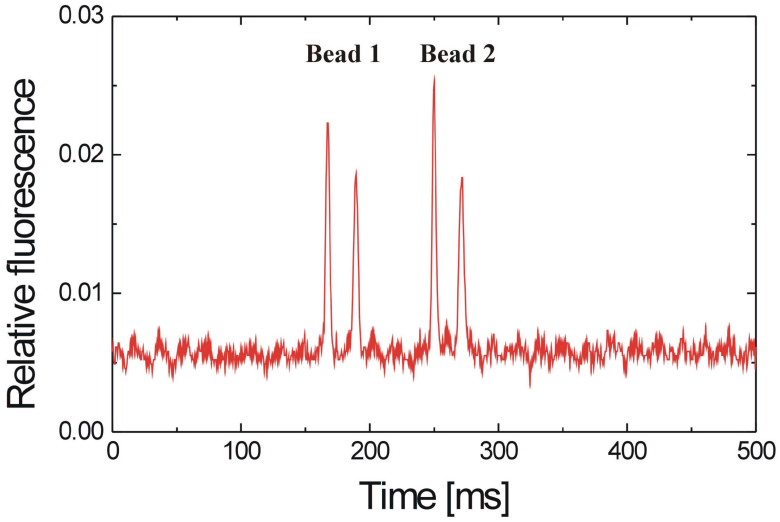

Figure 9.9: *Fluorescent signal as function of time from a flow cytometry setup where light is guided to the flow channel through a 1x2 splitter. The fluorescent signal is from two fluorescent beads flowing through the system.*

and x with x corresponding to ∼135ms or a velocity of ∼0.75mm/s. Compared to the experiment with a 1x2 split waveguide the signal-to-noise ratio is lower, only about ∼3 for two of the peaks. This is due to the high propagation loss at 488nm and to the losses that occur when the waveguides are split. At this wavelength, 1x4 splitters are only just functional. However, at wavelength above 600nm the performance of the splitters should be better.

9.5 Outlook

The simple fabrication process for the SU-8 based polymer waveguides offers great potential for future integration of planar waveguides in a number of μTAS devices. Furthermore, the fabrication process for the polymer waveguides is compatible with the PCR chip with integrated DEP based sample pretreatment system presented in this thesis.

In figure 9.11 a TWD device with integrated waveguides is shown. The fabrication of this structure is identical to the DEP devices presented in chapter 5 as the waveguides are simply defined in the same step as the fluidic system. In the device the the asymmetrically 1x4 splitter can be used to measure both the direction and the velocity of cells moved by TWD.

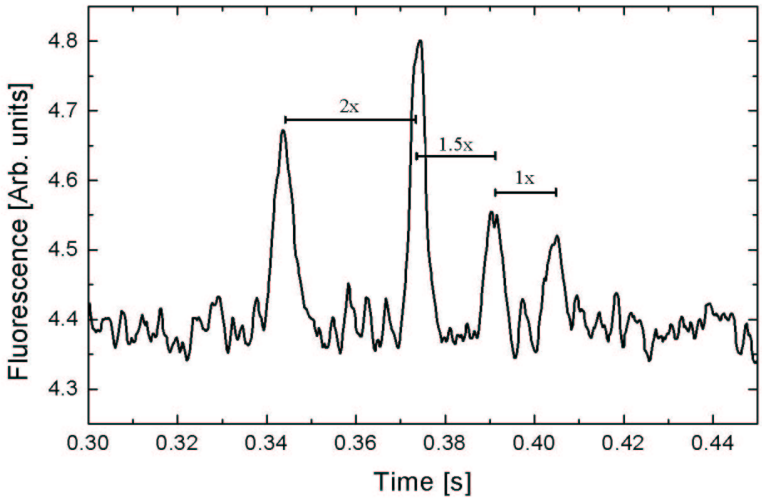

Figure 9.10: *Fluorescent signal as function of time from a flow cytometry setup where light is guided to the flow channel through a 1x4 asymmetrically splitter. The spacing of the peaks correspond to the the asymmetrical spacing of x, 1.5x and 2x between the waveguides.*

The ability to integrate waveguides without adding to the fabrication complexity is important. Increased fabrication complexity when integrating two devices often adds limitations to the integrated functionality.

As mentioned earlier integrated planar waveguides are also useful for real-time monitoring of PCR product. Although not realized yet, future integration of planar waveguides with the presented PCR chip with sample pretreatment system would be an important step towards the realization of a fully integrated μTAS.

9.6 Summary

In this chapter design and fabrication of planar polymer waveguides for use in μTAS devices has been presented. By defining the waveguides, fiber-to-waveguides couplers and the fluidic system in one single mask step fabrication and packaging of the devices could be done in a single day. The waveguides had a relatively high propagation loss at wavelengths below 550nm. However, above 550nm the loss is less than 3db/cm. The devices were tested in a flow cytometry setup using fluorescent beads. Even though the propagation loss at this wavelength is relatively high, excitation through 1x2 and 1x4 splitted waveguides using a 488nm Ar-ion laser was possible. However, the signal to noise ratio with 1x4 splitted waveguides was as low as 3. The SU-8 based waveguides can potentially also be integrated with the PCR chips and the cell handling devices presented in this thesis, without adding to the fabrication complexity.

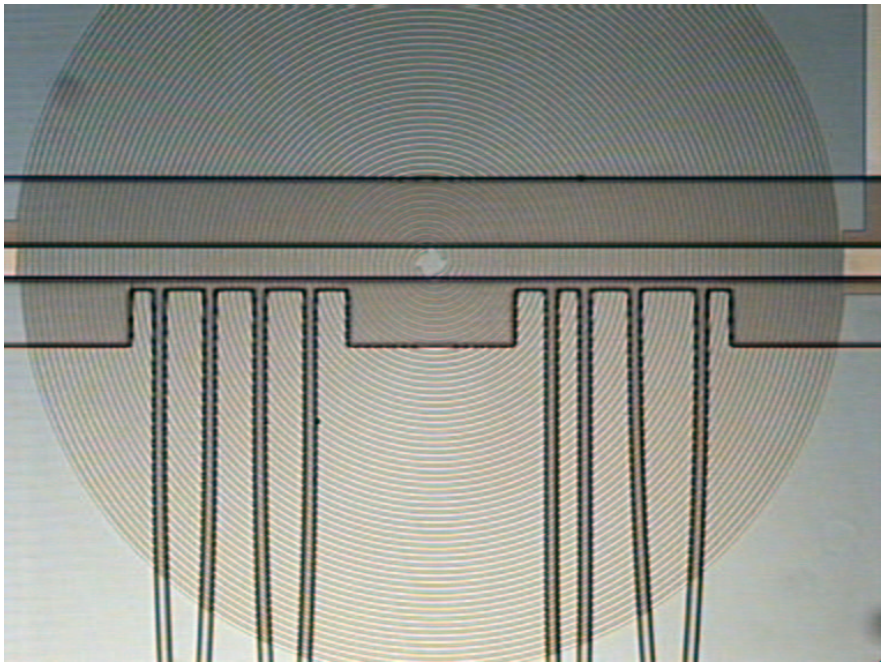

Figure 9.11: *Optical image of spiral type TWD device integrated with SU-8 based polymer waveguides. When a fluorescent particle passes in front of one of the waveguides there will be peak in the fluorescent signal. The time between the peaks in the fluorescent signal is then a measure of the velocity of the particle.*

Chapter 10

Conclusions

The major goal of this thesis has been to design and fabricate a PCR thermocycling chip with integrated DEP based sample pretreatment. The integration was successfully achieved by development of designs that used the photoresist SU-8 to define all the fluidic components of the systems on glass substrates.

The PCR functionality of the integrated chip was based on a PCR chip design with a SU-8 PCR chamber fabricated on a glass substrate. Integrated thin film heater and temperature sensor electrodes controlled the PCR thermocycling. A uniform temperature distribution in the PCR chamber was obtained by optimizing the heater configuration using FEM simulations. It was found that the heater spacing should be 100μm and that the heaters should continue beneath and beyond the PCR chamber walls. A second version of the PCR chip had to be designed and fabricated, when it was discovered that the original heater configuration had a negative impact on the temperature readout of the build in thermometer. Simulations showed that the design could function on glass substrates with thicknesses in the region from 500μm to 1500μm. A 1000μm borosilicate substrate was chosen because it represented a good compromise between power consumption and obtainable cooling rates.

Simulations and measurements showed that the PCR chip design was capable of fast thermocycling with heating and cooling rates in excess of 50°C/s and 30°C/s, respectively. The power consumption at a typical denaturation temperature of 94°C was measured to be 5.7W corresponding to predictions from the thermal modelling of the PCR chip.

Experiments showed it was necessary to enhance the PCR compatibility of the PCR chamber surfaces by silanization. The yield of PCR product in silanized chips was found to be ∼2/3 of the yield in conventional tubes when performed under identical conditions. Even when thermocycling faster than possible with conventional thermocyclers was used, the yield of the PCR chips was still comparable with the yield from the slower cycled conventional PCR tubes.

The DEP functionality of the integrated chip was based on designs with silicide electrodes fabricated on various substrates with a simple SU-8 fluidic system. Titanium and nickel silicide was chosen as electrode material because they offered the possibility for high performing and corrosion resistant electrodes suitable for operation in electrolyte solutions. Test designs for both the cell capture technique and travelling wave dielectrophoresis (TWD) were fabricated.

Experiments with DEP structures on silicon substrates validated various cell manipulation techniques including potential sample pretreatment functionality like separation and up-concentration of cells. The sample pretreatment functionality could be obtained using both cell capture and TWD structures.

Fabrication of high quality titanium silicide electrodes on glass substrates proved difficult. The electrodes suffered from cracks and flaking when fabricated on fused silica substrates, presumably due to thermally induced stress caused by the large mismatch in the coefficients of thermal expansion (CTE) between fused silica and titanium silicide. Nickel silicide is formed at a lower temperature than titanium silicide and is therefore less affected by thermal induced stress. High quality nickel silicide electrodes could thus be fabricated on both fused silica as well as on borosilicate glass substrates.

It was decided to use a cell capture type sample pretreatment system based on nickel silicide electrodes in the integrated PCR chip. The fluidic system that connects the sample pretreatment system with the PCR chamber allows for sample pretreatment to be performed in a separate medium than the medium used for PCR amplification. After the sample pretreatment the cells can be transported to the PCR chamber and mixed with PCR mastermix without changing the content of the mastermix radically. Two versions of the integrated PCR chip has been fabricated. Version I was fabricated on 500μm fused silica substrates and used platinum thin film electrodes to control the PCR thermocycling. Version II was fabricated on 1000μm borosilicate substrates and used nickel silicide electrodes both in the DEP based sample pretreatment system and to control the PCR thermocycling. The fabrication process for version II of the integrated chip is simpler than version I.

In agrement with the thermal simulations the power consumption and the cooling rates of chip version I fabricated on 500μm fused silica substrates were higher than for chip version II fabricated on 1000μm borosilicate substrates. The power consumption at 94°C was measured to be 7.0W for chip version I and 3.3W for chip version II. Cooling rates of up to $\sim$ 100°C/s have been measured for chips version I fabricated on 500μm fused silica substrates, while chips fabricated on 1000μm borosilicate substrates could achieve cooling rates of up to $\sim$ 30°C/s. However, both power consumption and cooling rates were found to be very dependent on the contact between the chip and the heatsink, especially for chips fabricated on 500μm fused silica substrates. A $\sim$ 50μm thick cyanoacrylate based adhesive layer was found to reduce both the power consumption and the cooling rates with more than 50% for chip version I. The effect on chip version II fabricated on 1000μm borosilicate substrates was found to be smaller

in agrement with thermal simulations. An adhesive with larger thermal conductivity should be used instead of the cyanoacrylate based adhesive to avoid the significant reduction in the thermal performance of the chips.

The testing of the integrated PCR chip is still in the initial stages. The basic functionality of the fluidic system has been characterized by releasing captured yeast cells and transporting them to the PCR chamber. To test the ability for sample pretreatment in the integrated chip, a mixture of yeast cells with a known amount of heparin was used. Heparin is PCR inhibiting and it was found that only the treated sample was successfully amplified.

As a step towards true μTAS with higher level of integration than the current PCR chip, SU-8 based polymer waveguides have been developed using a fabrication process compatible with the integrated PCR chip. In the design the waveguides, the fluidic system and fiber-to-waveguide couplers were defined using a single mask step, thus ensuring self-alignment between the optics and the fluidics. The waveguides had a relatively high propagation loss at wavelengths below 550nm. However, above 550nm the loss was less than 3db/cm. The functionality of the waveguides were tested in a flow cytometry setup using fluorescent beads.

The area of sample pretreatment is still under development and it remains one of the main challenges in the development of true μTAS. Although the presented PCR chip is not able to function with all "real world" samples, it is capable of performing many of the typical sample pretreatment steps needed prior to PCR on chip. Furthermore, the SU-8 based design makes future integration of other functionality, like CE or SU-8 planar waveguides for optical detection possible. It is therefore believed that the presented integrated PCR chip could mark a first step on a long road which eventually can lead to the development of a true μTAS.

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Appendix A

List of publications

Accepted or submitted peer-reviewed journal and conference papers.

- J. El-Ali, I.R. Perch-Nielsen, C.R. Poulsen, P.Telleman, A. Wolff, "SU-8 based PCR chip with integrated heaters and thermometor", Eurosensors XVI, Prauge, Czech Republic, September, 2002, p277-278. Oral presentation.
- J. El-Ali, K.B. Mogensen, I.R.P Nielsen, J.P. Kutter, P. Telleman and A. Wolff, "Integration of polymer waveguides for optical detection in biochemical microsystems", μ-TAS 2002, Nara, Japan, November, 2002, p.260-262. Poster presentation.
- J. El-Ali, I.R. Perch-Nielsen, C.R. Poulsen, D.D. Bang, P.Telleman, A. Wolff, "Simulation and experimental validation of a SU-8 based PCR thermocycler chip with integrated heaters and temperature sensor". Submitted to Sensors and Actuators.
- K.B. Mogensen, J. El-Ali, A. Wolff, J.P. Kutter, "Integration of polymer waveguides for optical detection in microfabricated chemical analysis systems". Submitted to Applied Optics.
- K.B. Mogensen, J. El-Ali, A. Wolff, J.P. Kutter, "Integrated Polymer Waveguides for Absorbance Detection in Chemical Analysis Systems", Transducer 03, Boston, USA, 2003. Accepted for poster presentation.
- J. El-Ali, I.R. Perch-Nielsen, C.R. Poulsen, M. Jensen, P.Telleman and A. Wolff, "Microfabricated DNA amplification device monolithically integrated with advanced sample pre-treatment", Transducer 03, Boston, USA, 2003. Accepted for oral presentation.

Appendix B

Process sequence for PCR chip

Wafers: 4" 1000μm thick Borofloat glass wafers from Schott [84].

1. **Cleaning of wafers:** Clean on turn-table using Triton X100 soap. Rinse 10 minutes in piranha (4:1 H_2SO_4:H_2O_2).

2. **Aluminum resist adhesion layer:** Deposit 20nm aluminum on the glass wafers using e-beam evaporation (Alcatel or Leybold).

3. **Spinning of resist for lift-off mask:** Dehydrate wafers in 120°C oven for ∼1 Hour. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.

4. **Photolithography:** UV exposure through metallization mask (mask 1). KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.

5. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.

6. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

7. **Removal of exposed aluminum:** Remove any exposed aluminium from the resist adhesion layer not removed during development of the resist in the aluminum etch (2:1 H_3PO_4:H_2O). Determine removal time by visual inspection during the etch.

8. **Deposition of platinum:** Bake resist on 120°C hotplate for 2 minutes. Deposit 200nm platinum using e-beam evaporation with a 100Å titanium adhesion layer. (Alcatel).

9. **Lift-off:** The platinum is lifted in a ultrasonic acetone bath for 5 minutes.

10. **Removal of remaining aluminum:** Remove the remaining aluminum from the resist adhesion layer in the aluminum etch (2:1 H_3PO_4:H_2O). Determine removal time by visual inspection during the etch.

11. **Spinning of SU-8 electrode protection layer:** Dehydrate wafers in 250°C oven for at least 3 Hours. Spin on 5μm SU-8 (XP2005, Microchem). KS-spinner:3000rpm, 30 seconds.

12. **Soft-baking of SU-8 protection layer :** Soft-bake the SU-8 on 90°C hotplate for 3.5 minutes (KS-spinner, bake program SU-8 thin).

13. **Photolithography:** UV exposure through protection mask (mask 2). KS aligner settings: 35 seconds exposure time, constant power of 275W , proximity mode 25μm.

14. **Post exposure bake:** Bake wafers on 95°C hotplate for 8 minutes with a 5 minutes ramp. Ramp temperature to 105°C using a 2 minute ramp. Bake at 105°C for 10 minutes. Let wafers cool down on hotplate.

15. **Spinning of SU-8 layer 1 for PCR chamber definition:** Spin on 200μm SU-8 (XP2075, Microchem). KS-spinner:1000rpm, 30 seconds.

16. **Soft-baking of SU-8 layer 1 for PCR chamber definition:** Soft-bake the SU-8 on 95°C hotplate for 45 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

17. **Spinning of SU-8 layer 2 for PCR chamber definition:** Spin on 200μm SU-8 (XP2075, Microchem). KS-spinner:1000rpm, 30 seconds.

18. **Soft-baking of SU-8 layer 2 for PCR chamber definition:** Soft-bake the SU-8 on 95°C hotplate for 45 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

19. **Photolithography:** UV exposure through PCR chamber mask (mask 3). KS aligner settings: Multiple exposure , 10 cycles of 14 seconds exposure 10 seconds wait, constant power of 275W, soft contact mode.

20. **Post exposure bake:** Bake wafers on 95°C hotplate for 35 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

21. **Development of SU-8:** Develop wafers in PGMEA: 25 minutes in developer labelled SU-8 first, 5 minutes in developer labelled SU-8 final. Rinse in isopropanol solution.

Appendix C

Process sequences for DEP structures

Titanium silicide electrodes on silicon substrates

Wafers: 4" 525μm thick single side polished silicon wafers.

1. **Deposition of LPCVD nitride:**. Process recipe SIRICH: LPCVD low stress nitride: 90 sccm SiH_2Cl_2, 16 sccm NH_3, 112 mTorr, 835°C, deposition time: 7 Hours. Nitride thickness $\sim$2μm.

2. **Deposition of LPCVD polysilicon:** Process recipe: Tamorph: 80 sccm Silane, 250 mTorr, 580°C. Deposition time: 40 minutes, Polysilicon thickness $\sim 180nm$.

3. **Spinning of resist for lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 1 minute on 90°C hotplate.

4. **Photolithography:** UV exposure through electrode mask. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.

5. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for $\sim$30 seconds.

6. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for $\sim$60 seconds at 22°C.

7. **Deposition of titanium:** BHF dip for 30 seconds. Deposit 80nm titanium using e-beam evaporation. (Alcatel).

8. **Lift-off:** The titanium is lifted in a ultrasonic acetone bath for 10 minutes.

9. **Formation of silicide:** RTA, pyro temperature setting, annealing time 1 minute, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 625°C. The temperature in polysilicon layer is higher (presumably T >800°C) than the temperature setting.

10. **Removal of excess silicon:** RIE, process:AB_ANISO, 40 sccm SF_6, 80 mTorr, 30 W, Etch time ∼50 sec. The etched time is controlled by an end-point signal.

11. **Removal of excess titanium:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

Nickel silicide electrodes on silicon substrates

Wafers: 4" 525μm thick single side polished silicon wafers.

1. **Deposition of LPCVD nitride:**. Process recipe SIRICH: LPCVD low stress nitride: 90 sccm SiH_2Cl_2, 16 sccm NH_3, 112 mTorr, 835°C, deposition time: 7 Hours. Nitride thickness ∼2μm.

2. **Deposition of LPCVD polysilicon:** Process recipe: Tamorph: 80 sccm Silane, 250 mTorr, 580°C. Deposition time: 40 minutes, Polysilicon thickness $\sim 180nm$.

3. **Spinning of resist for lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, softbake for 2 minutes on 90°C hotplate.

4. **Photolithography:** UV exposure through electrode mask. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.

5. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.

6. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

7. **Deposition of nickel:** BHF dip for 30 seconds. Deposit 80nm nickel using e-beam evaporation. (Alcatel or Leybold).

8. **Lift-off:** The nickel is lifted in a ultrasonic acetone bath for 10 minutes.

9. **Formation of silicide:** RTA, thermocouple temperature setting, annealing time 15 minute, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 425°C. The temperature in polysilicon layer is presumably higher than the temperature setting.

10. **Removal of excess silicon:** KOH, 60°C. The etch time is controlled by visual inspection during the etch.

11. **Rinse and removal of excess nickel:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

Silicide DEP devices

Wafers: 4" 525μm thick single side polished silicon wafers.

1. **Form silicide electrodes:** The silicide electrodes are formed using either the titanium or nickel silicide electrode process described previously in this appendix.
2. **Spinning of SU-8 layer for fluidic system:** Dehydrate wafers in 250°C oven for at least 3 Hours. Spin on 75μm SU-8 (XP2075, Microchem). KS-spinner:3000rpm, 30 seconds.
3. **Soft-baking of SU-8 layer :** Soft-bake the SU-8 on 95°C hotplate for 15 minutes with a 5 minutes ramp. Let wafers cool on a non-metallic surface.
4. **Photolithography:** UV exposure through fluidic system mask. KS aligner settings: Multiple exposure , 10 cycles of 10 seconds exposure 10 seconds wait, constant power of 275W, soft contact mode.
5. **Post exposure bake:** Bake wafers 95°C hotplate for 20 minutes with a 5 minutes ramp. Let wafers cool down on hotplate.
6. **Development of SU-8:** Develop wafers in PGMEA: 8 minutes in developer labelled SU-8 first, 2 minutes in developer labelled SU-8 final. Rinse in isopropanol solution.

Thick titanium silicide electrodes on fused silica substrates

Wafers: 4" 500μm fused silica wafers from Hoya [103].

1. **Deposition of LPCVD polysilicon:** Process recipe: Tamorph: 80 sccm Silane, 250 mTorr, 580°C. Deposition time: 40 minutes, Polysilicon thickness $\sim 180nm$.
2. **Spinning of resist for lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.
3. **Photolithography:** UV exposure through electrode mask. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.
4. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.
5. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.
6. **Deposition of titanium:** BHF dip for 30 seconds. Deposit 80nm titanium using e-beam evaporation. (Alcatel).

7. **Lift-off:** The titanium is lifted in a ultrasonic acetone bath for 10 minutes.

8. **Formation of silicide:** RTA, pyro temperature setting, annealing time 2 minutes, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 775°C. Place wafer between two silicon wafers (with oxide coatings) to avoid direct heating of polysilicon layer.

9. **Removal of excess titanium:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

Thin titanium silicide electrodes on fused silica substrates

Wafers: 4" 500μm fused silica wafers from Hoya [103].

1. **Deposition of LPCVD polysilicon:** Process recipe: Tamorph: 80 sccm Silane, 250 mTorr, 580°C. Deposition time: 22 minutes, Polysilicon thickness $\sim 100nm$.

2. **Spinning of resist for lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.

3. **Photolithography:** UV exposure through electrode mask. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.

4. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.

5. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

6. **Deposition of titanium:** BHF dip for 30 seconds. Deposit 35nm titanium using e-beam evaporation. (Alcatel).

7. **Lift-off:** The titanium is lifted in a ultrasonic acetone bath for 10 minutes.

8. **Formation of silicide:** RTA, pyro temperature setting, annealing time 2 minutes, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 775°C. Place wafer between two silicon wafers (with oxide coatings) to avoid direct heating of polysilicon layer.

9. **Removal of excess titanium:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

Nickel silicide electrodes on fused silica substrates

Wafers: 4" 500μm fused silica wafers from Hoya [103].

1. **Deposition of LPCVD polysilicon:** Process recipe: Tamorph: 80 sccm Silane, 250 mTorr, 580°C. Deposition time: 22 minutes, Polysilicon thickness $\sim 100nm$.
2. **Spinning of resist for lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.
3. **Photolithography:** UV exposure through electrode mask. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.
4. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.
5. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.
6. **Deposition of nickel:** BHF dip for 30 seconds. Deposit 60nm nickel using e-beam evaporation. (Alcatel).
7. **Lift-off:** The nickel is lifted in a ultrasonic acetone bath for 10 minutes.
8. **Formation of silicide:** RTA, thermocouple temperature setting, annealing time 15 minutes, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 425°C.
9. **Removal of excess nickel:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

Nickel silicide electrodes on borosilicate substrates

Wafers: 4" 1000μm borosilicate wafers from Schott [84].

1. **Deposition of sputtered silicon:** Sputter deposit 100nm silicon using Varian DC magnatron sputter.
2. **Spinning of resist for lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.
3. **Photolithography:** UV exposure through electrode mask. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.
4. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.
5. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

6. **Deposition of nickel:** BHF dip for 30 seconds. Deposit 60nm nickel using e-beam evaporation. (Alcatel).

7. **Lift-off:** The nickel is lifted in a ultrasonic acetone bath for 10 minutes.

8. **Formation of silicide:** RTA, thermocouple temperature setting, annealing time 15 minutes, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 425°C.

9. **Removal of excess nickel:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

Appendix D

Process sequences for integrated PCR chips

Integrated PCR chip Version I: Fused silica substrates

Wafers: 4" 500μm fused silica wafers from Hoya [103].

1. **Deposition of LPCVD polysilicon:** Process recipe: Tamorph: 80 sccm Silane, 250 mTorr, 580°C. Deposition time: 22 minutes, Polysilicon thickness $\sim 100nm$.

2. **Spinning of resist for DEP electrode lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.

3. **Photolithography:** UV exposure through DEP electrode mask, mask 1. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.

4. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.

5. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

6. **Deposition of nickel:** BHF dip for 30 seconds. Deposit 60nm nickel using e-beam evaporation. (Alcatel).

7. **Lift-off:** The nickel is lifted in a ultrasonic acetone bath for 10 minutes.

8. **Formation of silicide:** RTA, thermocouple temperature setting, annealing time 15 minutes, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 425°C.

9. **Removal of excess nickel:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

10. **Spinning of resist for polysilicon etch mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.

11. **Photolithography:** UV exposure through electrode protection mask, mask 3. KS aligner settings: 10 second exposure time, constant power of 275W , soft contact mode.

12. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

13. **Bake resist:** The resist is baked on the 120°C hotplate for 2 minutes.

14. **Removal of exposed polysiliconm:** Etch in polysilicon etch (20:1:20 HNO_3:HF:H_2O). The etch time is controlled by visual inspection during the etch.

15. **Strip of resist mask:** The resist is stripped in acetone for 5 minutes.

16. **Spinning of resist for PCR electrode lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, softbake for 2 minutes on 90°C hotplate.

17. **Photolithography:** UV exposure through PCR electrode mask, mask 2. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.

18. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.

19. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

20. **Deposition of platinum:** Deposit 150nm platinum with a 100Å titanium adhesion layer using e-beam evaporation. (Alcatel).

21. **Lift-off:** The platinum is lifted in a ultrasonic acetone bath for 5 minutes.

22. **Spinning of SU-8 electrode protection layer:** Dehydrate wafers in 250°C oven for at least 3 Hours. Spin on 5μm SU-8 (XP2005, Microchem). KS-spinner:3000rpm, 30 seconds.

23. **Soft-baking of SU-8 protection layer :** Soft-bake the SU-8 on 90°C hotplate for 3.5 minutes (KS-spinner, bake program SU-8 thin).

24. **Photolithography:** UV exposure through protection mask (mask 3). KS aligner settings: 35 seconds exposure time, constant power of 275W , proximity mode 25μm.

25. **Post exposure bake:** Bake wafers 95°C hotplate for 8 minutes with a 5 minutes ramp. Ramp temperature to 105°C using a 2 minute ramp. Bake at 105°C for 10 minutes. Let wafers cool down on hotplate.

26. **Spinning of SU-8 layer 1 for PCR chamber and fluidic system definition:** Spin on 200μm SU-8 (XP2075, Microchem). KS-spinner:1000rpm, 30 seconds.

27. **Soft-baking of SU-8 layer 1 for PCR chamber and fluidic system definition:** Soft-bake the SU-8 on 95°C hotplate for 45 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

28. **Spinning of SU-8 layer 2 for PCR chamber and fluidic system definition:** Spin on 200μm SU-8 (XP2075, Microchem). KS-spinner:1000rpm, 30 seconds.

29. **Soft-baking of SU-8 layer 2 for PCR chamber and fluidic system definition:** Soft-bake the SU-8 on 95°C hotplate for 45 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

30. **Photolithography:** UV exposure through fluidic system definition mask (mask 4). KS aligner settings: Multiple exposure , 10 cycles of 14 seconds exposure 10 seconds wait, constant power of 275W, soft contact mode.

31. **Post exposure bake:** Bake wafers 95°C hotplate for 35 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

32. **Development of SU-8:** Develop wafers in PGMEA: 25 minutes in developer labelled SU-8 first, 5 minutes in developer labelled SU-8 final. Rinse in isopropanol solution.

Integrated PCR chip Version II: Borosilicate substrates

Wafers: 4" 1000μm Borofloat wafers from Schott [84].

1. **Deposition of sputtered silicon:** Sputter deposit 100nm silicon using Varian DC magnatron sputter.

2. **Spinning of resist for the combined DEP and PCR electrode lift-off mask:** HMDS treatment for 30 minutes. Spin on 1.5μm AZ5214 photoresist, soft-bake for 2 minutes on 90°C hotplate.

3. **Photolithography:** UV exposure through combined DEP and PCR electrode mask. KS aligner settings: 7 second exposure time, constant power of 275W , soft contact mode.

4. **Image reversal:** Bake resist on 120°C hotplate for 2 minutes. UV flood exposure wafers for ∼30 seconds.

5. **Development of resist:** Develop wafers in a 1 AZ 351B : 5 DI water solution for ∼60 seconds at 22°C.

6. **Deposition of nickel:** BHF dip for 30 seconds. Deposit 60nm nickel using e-beam evaporation. (Alcatel).

7. **Lift-off:** The nickel is lifted in a ultrasonic acetone bath for 10 minutes.

8. **Formation of silicide:** RTA, thermocouple temperature setting, annealing time 15 minutes, maximum argon flow for at least 7 minutes prior to anneal, temperature setting 425°C.

9. **Removal of excess nickel:** piranha (4:1 H_2SO_4:H_2O_2), 10 minutes.

10. **Spinning of SU-8 electrode protection layer:** Dehydrate wafers in 250°C oven for at least 3 Hours. Spin on 5μm SU-8 (XP2005, Microchem). KS-spinner:3000rpm, 30 seconds.

11. **Soft-baking of SU-8 protection layer :** Soft-bake the SU-8 on 90°C hotplate for 3.5 minutes (KS-spinner, bake program SU-8 thin).

12. **Photolithography:** UV exposure through protection mask (mask 3). KS aligner settings: 35 seconds exposure time, constant power of 275W , proximity mode 25μm.

13. **Post exposure bake:** Bake wafers 95°C hotplate for 8 minutes with a 5 minutes ramp. Ramp temperature to 105°C using a 2 minute ramp. Bake at 105°C for 10 minutes. Let wafers cool down on hotplate.

14. **Spinning of SU-8 layer 1 for PCR chamber and fluidic system definition:** Spin on 200μm SU-8 (XP2075, Microchem). KS-spinner:1000rpm, 30 seconds.

15. **Soft-baking of SU-8 layer 1 for PCR chamber and fluidic system definition:** Soft-bake the SU-8 on 95°C hotplate for 45 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

16. **Spinning of SU-8 layer 2 for PCR chamber and fluidic system definition:** Spin on 200μm SU-8 (XP2075, Microchem). KS-spinner:1000rpm, 30 seconds.

17. **Soft-baking of SU-8 layer 2 for PCR chamber and fluidic system definition:** Soft-bake the SU-8 on 95°C hotplate for 45 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

18. **Photolithography:** UV exposure through fluidic system definition mask (mask 4). KS aligner settings: Multiple exposure , 10 cycles of 14 seconds exposure 10 seconds wait, constant power of 275W, soft contact mode.

19. **Post exposure bake:** Bake wafers 95°C hotplate for 35 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

20. **Development of SU-8:** Develop wafers in PGMEA: 25 minutes in developer labelled SU-8 first, 5 minutes in developer labelled SU-8 final. Rinse in isopropanol solution.

Appendix E

Process sequences for polymer waveguides

Wafers: 4" 525μm thick single side polished silicon wafers.

1. **Forming of waveguide buffer layer:** Thermal oxidation: Process wet1100, oxidation time: 16 hours, oxide thickness $\sim 2.5\mu$m.

2. **Spinning of SU-8 waveguide core and fluidic system layer layer:** Dehydrate wafers in 250°C oven for at least 3 Hours. Spin on 90μm SU-8 (XP2075, Microchem). KS-spinner:1800rpm, 30 seconds.

3. **Softbaking of SU-8 layer :** Softbake the SU-8 on 95°C hotplate for 25 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

4. **Photolithography:** UV exposure through waveguide mask. KS aligner settings: Multiple exposure , 10 cycles of 10 seconds exposure 10 seconds wait, constant power of 275W, soft contact mode.

5. **Post exposure bake:** Bake wafers 95°C hotplate for 25 minutes with a 10 minutes ramp. Let wafers cool down on hotplate.

6. **Development of SU-8:** Develop wafers in PGMEA: 8 minutes in developer labelled SU-8 first, 2 minutes in developer labelled SU-8 final. Rinse in isopropanol solution.